MULTI-INNO TECHNOLOGY CO., LTD.

LCD MODULE SPECIFICATION

Model : MI9664AO

Revision	
Engineering	
Date	
Our Reference	

Revised History

Part Number	Revision	Revision Content	Revised on
MI9664AO	A	New	Jan 11, 2006

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1. Basic Specifications

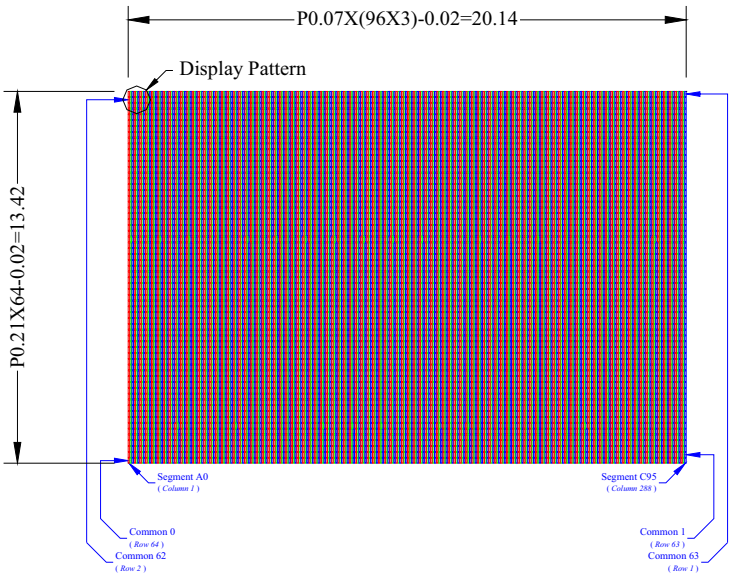
1.1 Display Specifications

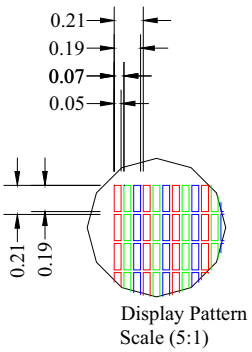
1) Display Mode: Passive Matrix
2) Display Color: 65,536 Colors (Maximum)
3) Drive Duty: 1/64 Duty

1.2 Mechanical Specifications

1) Outline Drawing: According to the annexed outline drawing number
2) Number of Pixels: 96(RGB) × 64
3) Panel Size: 27.20 × 21.50 × 1.60 (mm)
4) Active Area: 20.14 × 13.42 (mm)
5) Pixel Pitch: 0.07 × 0.21 (mm)
6) Pixel Size: 0.05 × 0.19 (mm)
7) Weight: 1.8 (g)

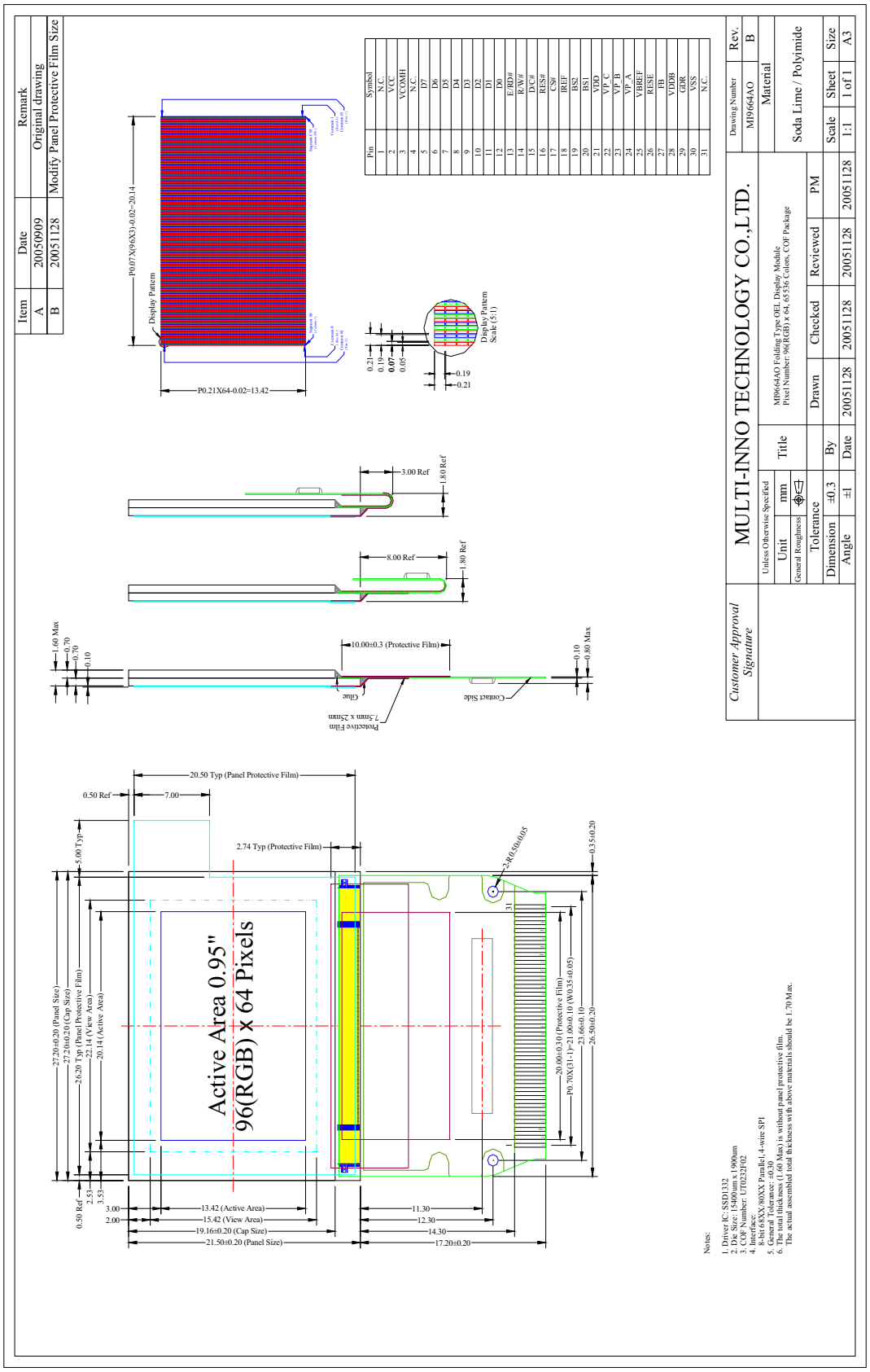
1.3 Active Area & Pixel Construction





Display Pattern
Scale (5:1)

1.4 Mechanical Drawing



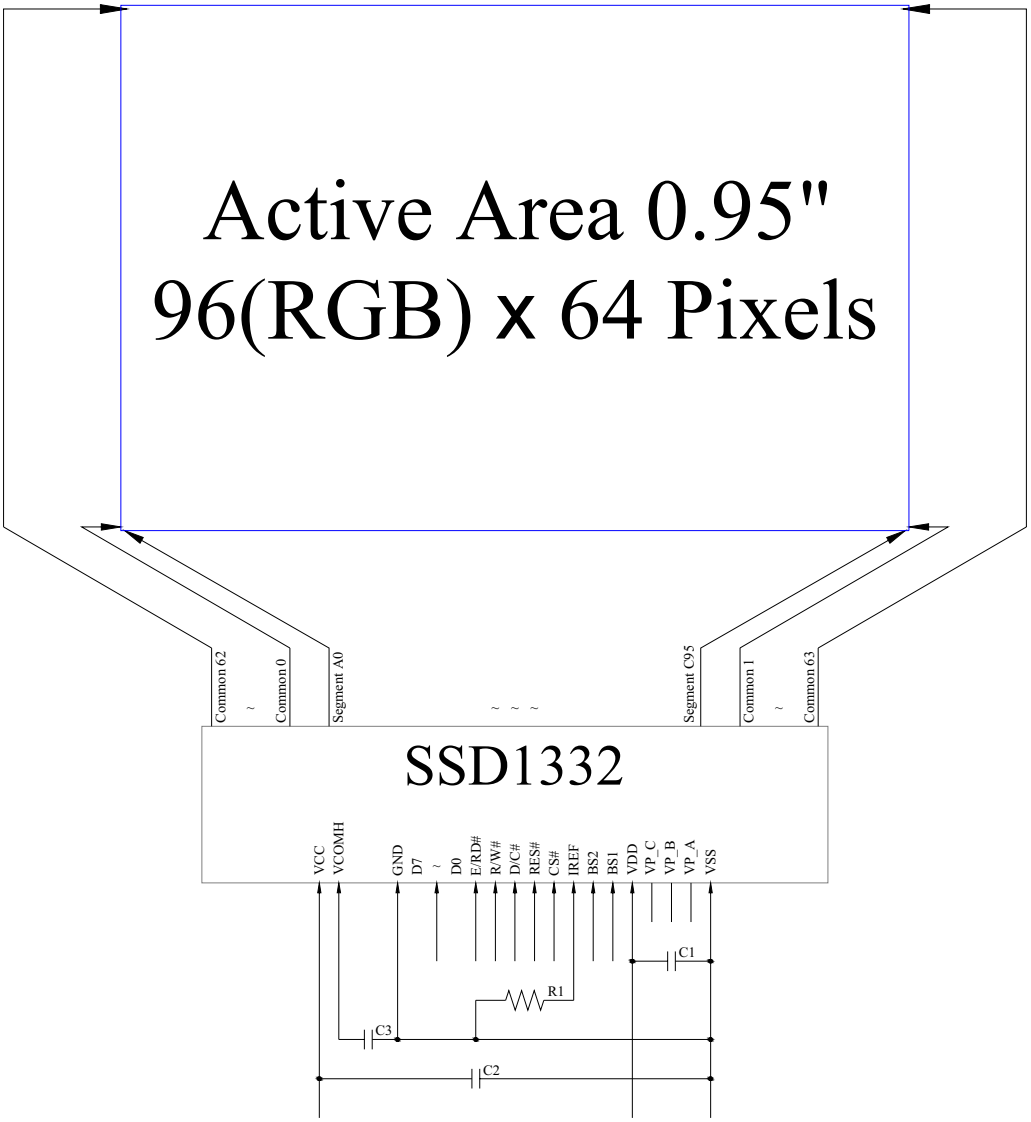
1.5 Pin Definition

<table>
<tr><th>Pin Number</th><th>Symbol</th><th>I/O</th><th>Function</th></tr>
<tr><td colspan="4">Power Supply</td></tr>
<tr><td>21</td><td>VDD</td><td>I</td><td>Power Supply for Logic Circuit
This is a voltage supply pin. It must be connected to external source.</td></tr>
<tr><td>30</td><td>VSS</td><td>I</td><td>Ground of OEL System
This is a ground pin. It also acts as a reference for the logic pins, the OEL driving voltages, and the analog circuits. It must be connected to external ground.</td></tr>
<tr><td>2</td><td>VCC</td><td>I/O</td><td>Power Supply for OEL Panel
This is the most positive voltage supply pin of the chip. It can be supplied externally or generated internally by using internal DC/DC voltage converter.</td></tr>
<tr><td colspan="4">Driver</td></tr>
<tr><td>24
23
22</td><td>VP_A
VP_B
VP_C</td><td>I</td><td>External Voltage Reference for Pre-charge Signal
These pins are the pre-charge driving voltages for OEL driving segment pins SA0~SA95, SB0~SB95 and SC0~SC95 respectively. They can be supplied externally or internally generated by VP circuit. When internal VP is used, VP_A, VP_B, VP_C pins should be left open.</td></tr>
<tr><td>18</td><td>IREF</td><td>I</td><td>Current Reference for Brightness Adjustment
This pin is segment current reference pin. A resistor should be connected between this pin and VSS. Set the current at 10uA.</td></tr>
<tr><td>3</td><td>VCOMH</td><td>I/O</td><td>Voltage Output High Level for COM Signal
This pin is the input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td colspan="4">Interface</td></tr>
<tr><td>20
19</td><td>BS1
BS2</td><td>I</td><td>Communicating Protocol Select
These pins are MCU interface selection input. See the following table:
<table>
<tr><td></td><td>68XX-parallel</td><td>80XX-parallel</td><td>Serial</td></tr>
<tr><td>BS1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>16</td><td>RES#</td><td>I</td><td>Power Reset for Controller and Driver
This pin is reset signal input. When the pin is low, initialization of the chip is executed.</td></tr>
<tr><td>17</td><td>CS#</td><td>I</td><td>Chip Select
This pin is the chip select input. The chip is enabled for MCU communication only when CS# is pulled low.</td></tr>
<tr><td>13</td><td>E/RD#</td><td>I</td><td>Read/Write Enable or Read
This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as the Enable (E) signal. Read/write operation is initiated when this pin is pulled high and the CS# is pulled low.
When connecting to an 80XX-microprocessor, this pin receives the Read (RD#) signal. Data read operation is initiated when this pin is pulled low and CS# is pulled low.</td></tr>
</table>

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Interface (Continued)			
14	R/W#	I	*Read/Write Select or Write* This pin is MCU interface input. When interfacing to a 68XX-series microprocessor, this pin will be used as Read/Write (R/W#) selection input. Pull this pin to "High" for read mode and pull it to "Low" for write mode. When 80XX interface mode is selected, this pin will be the Write (WR#) input. Data write operation is initiated when this pin is pulled low and the CS# is pulled low.
15	D/C#	I	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high, the input at D7~D0 is treated as display data. When the pin is pulled low, the input at D7~D0 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
5~12	D7~D0	I/O	*Host Data Input/Output Bus* These pins are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When serial mode is selected, D1 will be the serial data input SDIN and D0 will be the serial clock input SCLK.
Reserve			
1, 4,31	N.C.	-	*Reserved Pin (Supporting Pin)* The supporting pins can reduce the influences from stresses on the function pins. It must be connected to external ground.
25	VBREF	I	*Voltage Reference for DC/DC Converter Circuit* *This pin is the internal voltage reference of booster circuit. A stabilization capacitor, typ. 1μF, should be connected to VSS.*
26	RESE	I	*Input for Connected External NMOS* *This pin connects to the source current pin of the external NMOS of the booster circuit.*
27	FB	I	*Feedback Input for DC/DC Converter Circuit* *This pin is the feedback resistor input of the booster circuit. It is used to adjust the booster output voltage level (VCC).*
28	VDDB	I	*This is the power supply pin for the internal buffer of the DC-DC voltage converter. 3.5>=VDDB>=VDD*
29	GDR	O	*Output for Connected External NMOS* *This output pin drives the gate of the external NMOS of the booster circuit.*

1.6 Block Diagram



MCU Interface Selection: BS1 and BS2
Pins connected to MCU interface: D7~D0, E/RD#, R/W#, D/C#, RES#, and CS#
* VP_A, VP_B, VP_C would be left float.

C1, C3: 4.7µF
C2: 10µF
R1: 910kΩ, R1 = (Voltage at IREF - BGGND) / IREF

2. *Absolute Maximum Ratings*

2.1 Absolute Maximum Ratings

Parameter	Min	Max	Unit	Condition	Notes
Supply Voltage V_{DD}	-0.3	4.0	V	Ta=25˚C	1, 2
Driver Supply Voltage V_{CC}	0	15	V	Ta=25˚C	1, 2
Operating Temperature T_{OP}	-20	70	°C		-
Storage Temperature T_{STG}	-30	80	°C		-
Operating Life Time	10,000		Hrs	90 cd/m^2, 50%checkerboard	
Storage Life Time	20,000		Hrs	Ta=25˚C, 50%RH	

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

2.2 Regarding the Gradation

Although this module possesses the gradation function, respective gradation levels will vary depending on the production conditions etc. Also, the temperature range where the gradation function can be guaranteed will be -10°C~60°C.

3. Electrical Characteristics

3.1 DC Characteristics

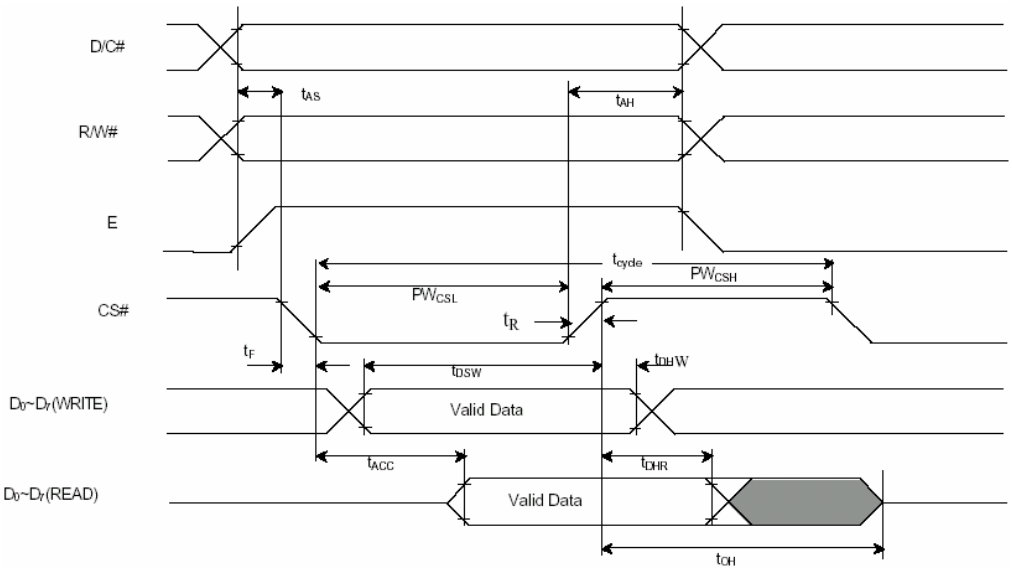
Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.5	2.8	3.5	V
Driver Supply Voltage	V_{CC}		-	11	-	V
High Level Input	V_{IH}	I_{out} = 100μA, 3.3MHz	0.8×V_{DD}	-	V_{DD}	V
Low Level Input	V_{IL}	I_{out} = 100μA, 3.3MHz	0	-	0.2×V_{DD}	V
High Level Output	V_{OH}	I_{out} = 100μA, 3.3MHz	0.9×V_{DD}	-	V_{DD}	V
Low Level Output	V_{OL}	I_{out} = 100μA, 3.3MHz	0	-	0.1×V_{DD}	V

3.2 AC Characteristics

3.2.1 68XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

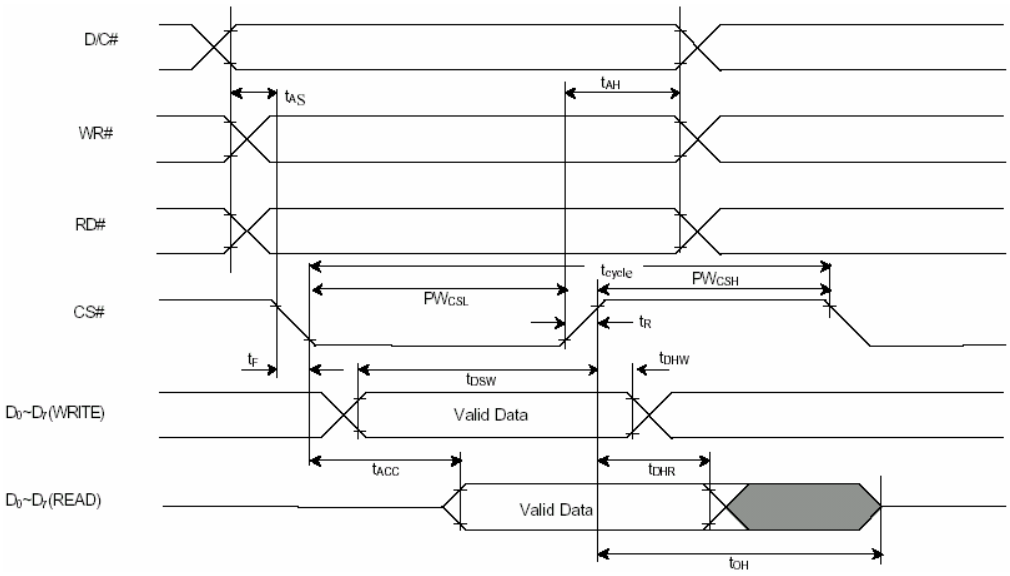
* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.2.2 80XX-Series MPU Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	ns
t_{AS}	Address Setup Time	0	-	ns
t_{AH}	Address Hold Time	0	-	ns
t_{DSW}	Write Data Setup Time	40	-	ns
t_{DHW}	Write Data Hold Time	15	-	ns
t_{DHR}	Read Data Hold Time	20	-	ns
t_{OH}	Output Disable Time	-	70	ns
t_{ACC}	Access Time	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (Read) Chip Select Low Pulse Width (Write)	120 60	-	ns
PW_{CSH}	Chip Select High Pulse Width (Read) Chip Select High Pulse Width (Write)	60 60	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

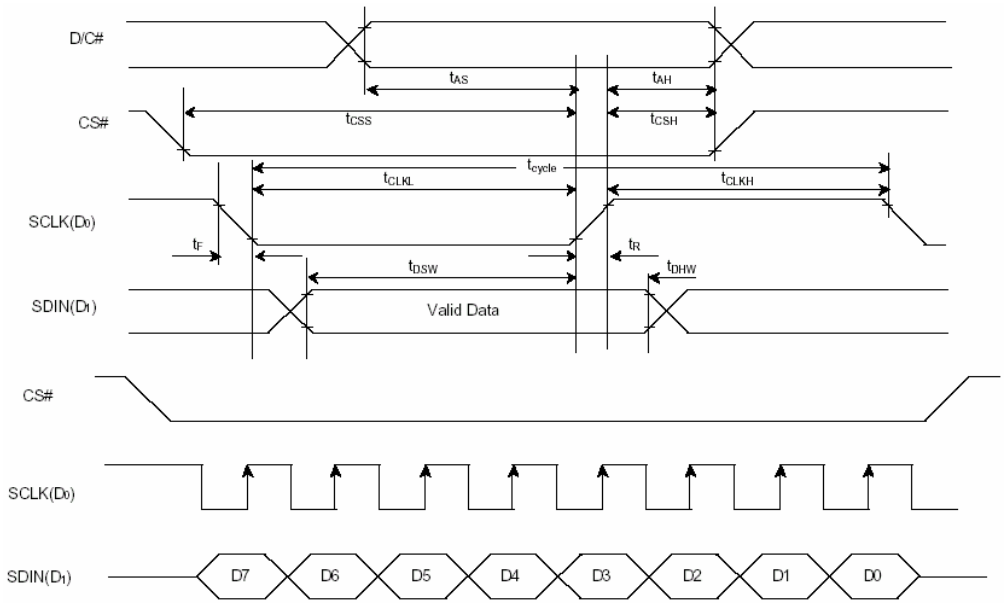
* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.2.3 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	ns
t_{AS}	Address Setup Time	150	-	ns
t_{AH}	Address Hold Time	150	-	ns
t_{CSS}	Chip Select Setup Time	120	-	ns
t_{CSH}	Chip Select Hold Time	60	-	ns
t_{DSW}	Write Data Setup Time	100	-	ns
t_{DHW}	Write Data Hold Time	100	-	ns
t_{CLKL}	Clock Low Time	100	-	ns
t_{CLKH}	Clock High Time	100	-	ns
t_R	Rise Time	-	15	ns
t_F	Fall Time	-	15	ns

* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.3 Optics & Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness (White)	L_{br}	Display Average (Note 4)	70	90	-	cd/m^2
C.I.E. (White)	(x) (y)		0.27 0.31	0.31 0.35	0.35 0.39	
C.I.E. (Red)	(x) (y)		0.61 0.29	0.65 0.33	0.69 0.37	
C.I.E. (Green)	(x) (y)		0.25 0.53	0.29 0.57	0.33 0.61	
C.I.E. (Blue)	(x) (y)		0.08 0.10	0.12 0.14	0.16 0.18	
Dark Room Contrast	CR		-	>1000:1	-	
Luminance Uniformity			-	>80	-	%
Response Time			-	<10		us
View Angle			-	>160	-	degree

Note 3: Optical measurement taken at 1/64 duty, 0x0A Master Current Setting

3.4 General Electrical Specification

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		2.5	2.8	3.5	V
Driver Supply Voltage	V_{CC}	Note 4		11		V
Operating Current for V_{DD}	I_{DD}	Note 5	-	0.2	0.3	mA
		Note 6	-	0.2	0.3	mA
Operating Current for V_{CC}	I_{CC}	Note 5	-	4.6	6.96	mA
		Note 6	-	15.8	23.7	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	1	-	µA
Sleep Mode Current for V_{CC}	$I_{CC, SLEEP}$		-	1	-	µA

Note 4: Brightness (L_{br}) and Driver Supply Voltage (V_{CC}) are subject to the change of the panel characteristics and the customer's request.

Note 5: V_{DD} = 2.8V, V_{CC} = 11V, Master Current Setting = 0x0A, 50% Display Area Turn on.

Note 6: V_{DD} = 2.8V, V_{CC} = 11V, Master Current Setting = 0x0A, 100% Display Area Turn on.

4. Functional Specification

4.1. Commands

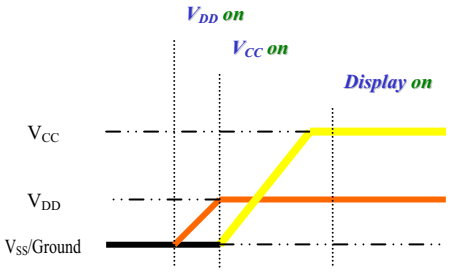
Refer to the Technical Manual for the SSD1332

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

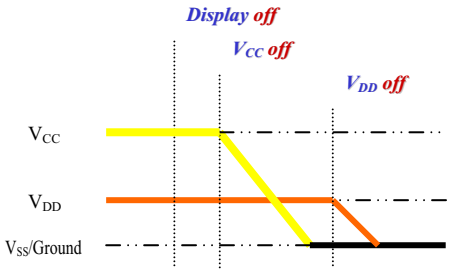
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Clear Screen
4. Power up V_{CC}
5. Delay 100ms
   (when V_{DD} is stable)
6. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{CC}
3. Delay 100ms
   (when V_{CC} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



4.3 Reset Circuit

When RES# input is low, the chip is initialized with the following status:

1. Display is OFF
2. 64 MUX Display Mode
3. Normal segment and display data column and row address mapping (SEG0 mapped to column address 00h and COM0 mapped to row address 00h)
4. Shift register data clear in serial interface
5. Display start line is set at display RAM address 0
6. Column address counter is set at 0
7. Normal scan direction of the COM outputs
8. Master current control register is set at 0Fh
9. Individual contrast control registers of color A, B, and C are set at 80h

4.4 Actual Application Example

Command usage and explanation of an actual example

<Initialization Setting>
Set Display Clock Divide Ratio / Oscillator Frequency
(10110011 with XXXXXXXX)

Set Display Offset
(10100010 with **XXXXXX)
* XXXXXX = 64 - Dummy Lines from Common 0
Set Multiplex Ratio
(10101000 with **XXXXXX)

Set Master Configuration
(10101101 with 10001XXX)
10001110 => 8Eh (External VCC Supply, Internal VCOMH Regulator & VP)

Set Display Start Line
(10100001 with **XXXXXX)
Set Segment Re-map & Data Format
(10100000 with XXXX**XX)
01100000 => 60h

Set Master Current Control
(10000111 with ****XXXX)
Set Contrast Control for Color A
(10000001 with XXXXXXXX)
Set Contrast Control for Color B
(10000010 with XXXXXXXX)
Set Contrast Control for Color C
(10000011 with XXXXXXXX)

Set VPA, VPB, VPC Level for Color A, B, C
(10111XXX with XXXXXXXX)
Set VCOMH
(10111110 with *XXXXXXX)

Set Phase 1 & 2 Period Adjustment
(10110001 with XXXXXXXX)
Set Power Save
(10110000 with 000X00X0)
00000000 => 00h (Normal)

Set Display Mode (101001XX)
10100100 => A4h (Normal)
Set Display On/Off (1010X111)
10101111 => AFh (Turns On)

<Display Boundary Setting>
Set Column Address
(00010101 with **XXXXXX for Start & **XXXXXX for End)
Set Row Address
(01110101 with ***XXXXX for Start & ***XXXXX for End)

If the noise is accidentally occurred at the displaying window during the operation, please reset the display in order to recover the display function.

5. *Reliability*

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	70°C, 240 hrs	The operational functions work.
Low Temperature Operation	-20°C, 240 hrs	
High Temperature Storage	80°C, 240 hrs	
Low Temperature Storage	-30°C, 240 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 120 hrs	
High Temperature/Humidity Storage	60°C, 90% RH, 240 hrs	
Thermal Shock	-40°C ⇔ 85°C, 24 cycles 60 mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure teat at 23±5°C; 55±15% RH.

6. *Outgoing Quality Control Specifications*

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15 %RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50 cm
Distance between the Panel & Eyes of the Inspector:	≥ 30 cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

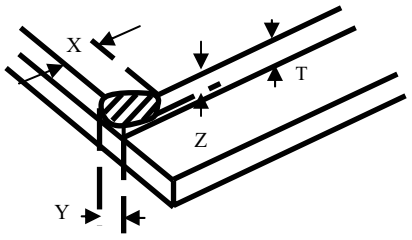
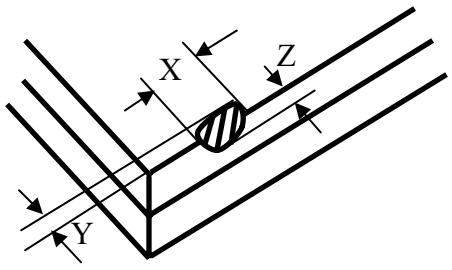
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

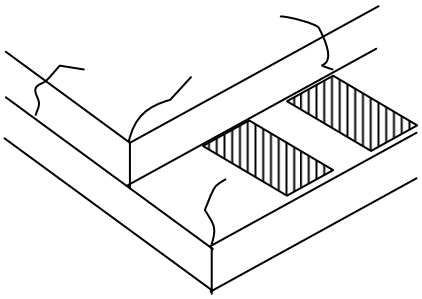
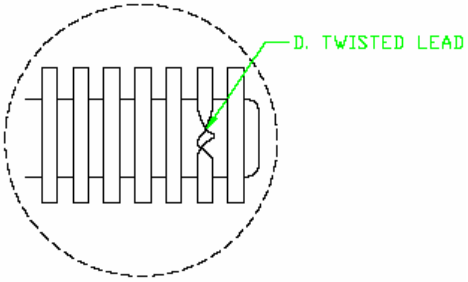
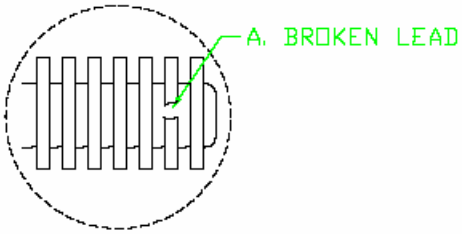
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

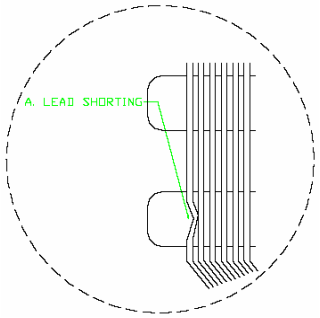
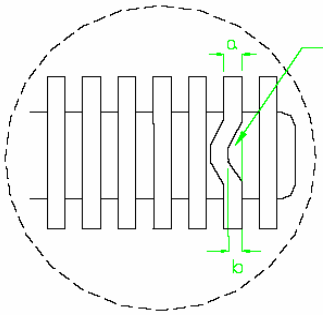
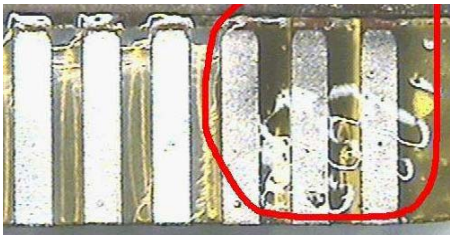
6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) Z ≤ T  

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Twist	Minor	Not Allowable 
Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Prober Mark	Acceptable	Ok

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

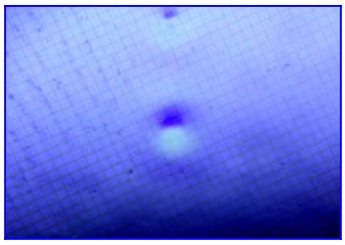
<table>
<tr><th>Check Item</th><th>Classification</th><th>Criteria</th></tr>
<tr><td rowspan="2">Terminal Lead Bent
(Not Twist or Broken)</td><td>Minor</td><td>NG if any bent lead cause lead shorting.
  </td></tr>
<tr><td>Minor</td><td>NG for horizontally bent lead more than 50% of its width.
  </td></tr>
<tr><td>Glue or Contamination on Pin
(Couldn’t Be Removed by Alcohol)</td><td>Minor</td><td>  </td></tr>
<tr><td>Ink Marking on Back Side of panel
(Exclude on Film)</td><td>Acceptable</td><td>Ignore for Any</td></tr>
</table>

6.3.2 Cosmetic Check (Display On) in Active Area

Don’t tear off the protective film for only visual check purpose. Otherwise any particle or contamination of air could penetrate & attach onto the surface of polarizer in great probability. It is recommended to execute in clear room environment (class 10k) if actual in necessary.

Check Item	Classification	Criteria	
Any Dirt & Scratch on Polarizer’s Protective Film	Acceptable	Ignore for not Affect the Polarizer	
Scratches, Fiber, Line-Shape Defect ** (On Polarizer)	Minor	W ≤ 0.05 W ≤ 0.1, L ≤ 2 2 < L	Ignore n ≤ 3 n = 0

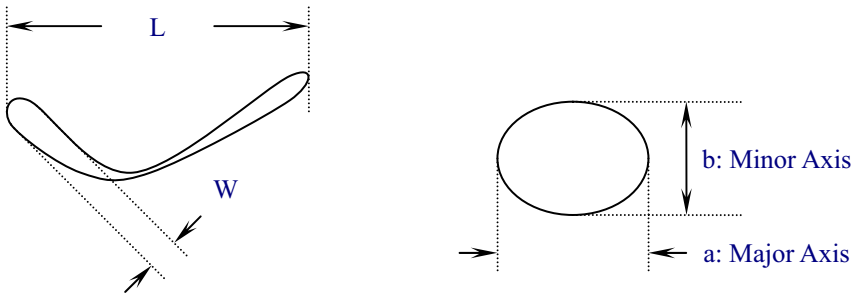
6.3.2 Cosmetic Check (Display On) in Active Area (Continued)

Check Item	Classification	Criteria
Dirt, Black Spot, Foreign Material, ** (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.2 n ≤ 3 0.2 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

* In displays which manifests itself has the other shadowing, ghosting or streaking.

** Distance between any 2 defects should over 10mm.

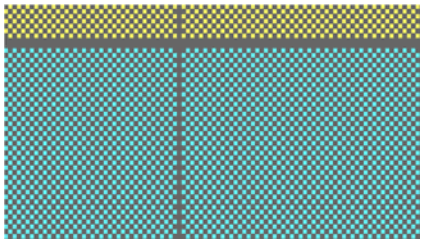
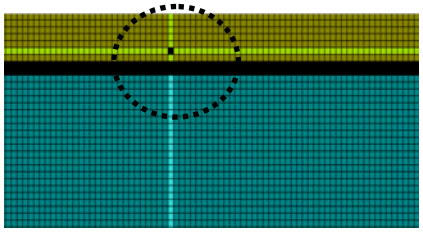
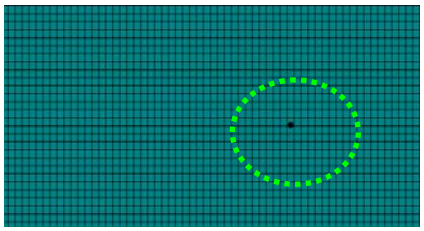
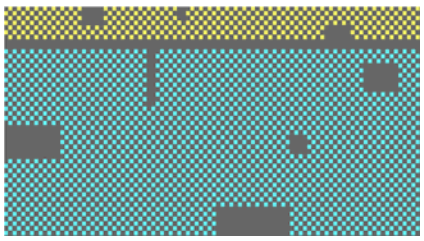
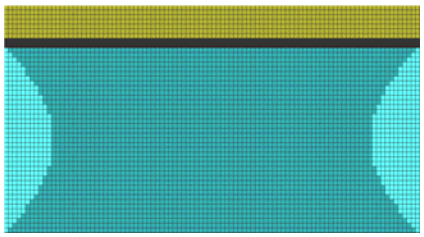
*** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



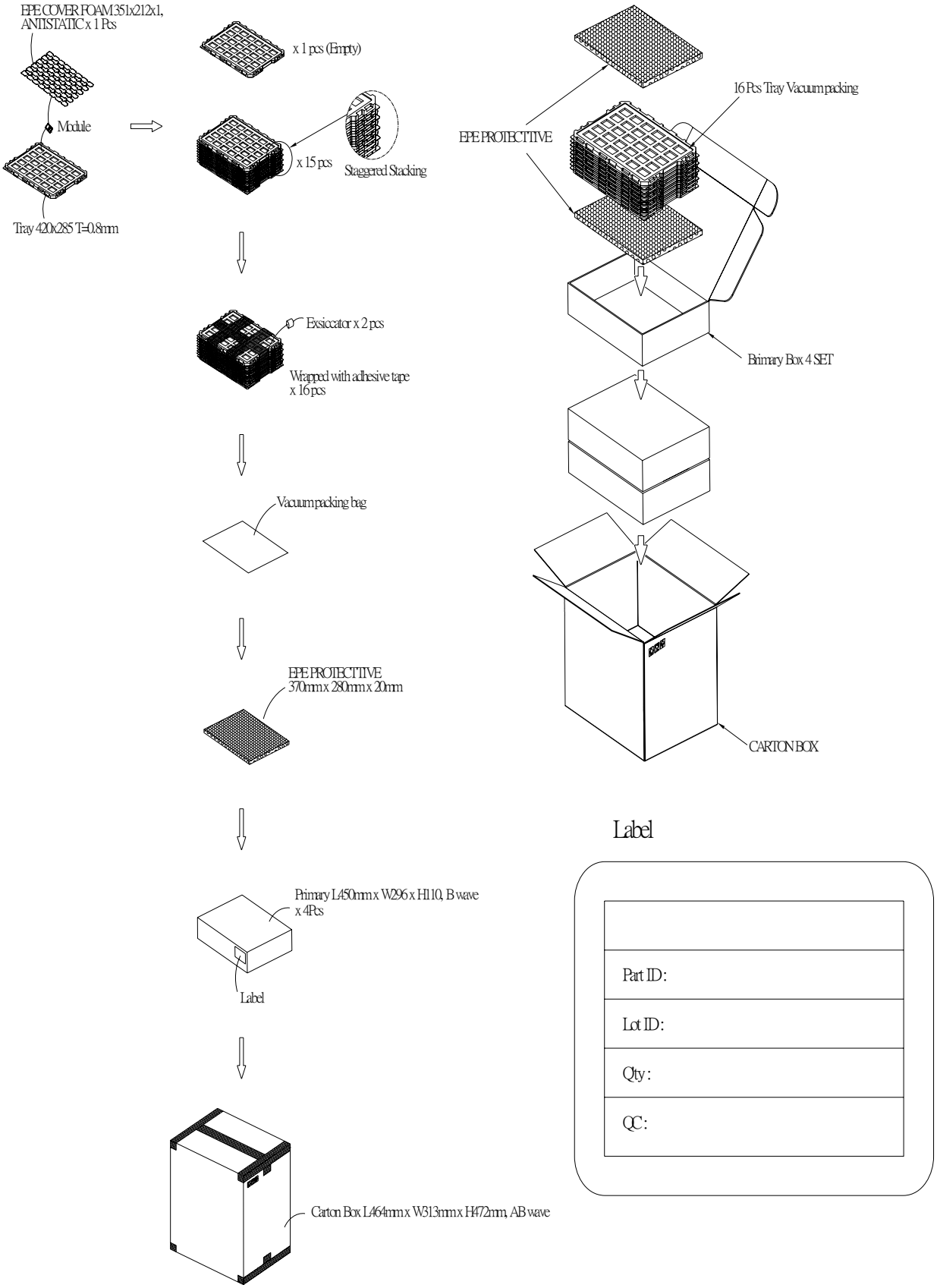
6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Flicker	Major	Not Allowable

6.3.3 Pattern Check (Display On) in Active Area (Continued)

Check Item	Classification	Criteria
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

7. Package Specifications



Label

Part ID:
Lot ID:
Qty:
QC:

8. *Precautions When Using These OEL Display Modules*

8.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) When installing the OEL display module, be careful not to apply twisting stress or deflection stress to the OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.
7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Multi-Inno Technology Co.,ltd.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: SSD1332
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.
2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the COF
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.