MULTI-INNO TECHNOLOGY CO., LTD.

LCD MODULE SPECIFICATION

Model : MI25664AO

Revision	
Engineering	
Date	
Our Reference	

Revised History

Part Number	Revision	Revision Content	Revised on
MI25664AO	A	New August 30, 2005	
	B	Page 11 Update Sec. 3.3 Optics Characteristic Page 11 Update Sec. 3.4 General Electrical Specification Page 13 Update Content of Sec. 5.2 Lifetime Page 13 Update sec 5.1 Contents of Reliability Tests Page 16~17 Update sec 6.3.1~6.3.2 Cosmetic Check	May 12, 2006

Contents

1. Basic Specifications

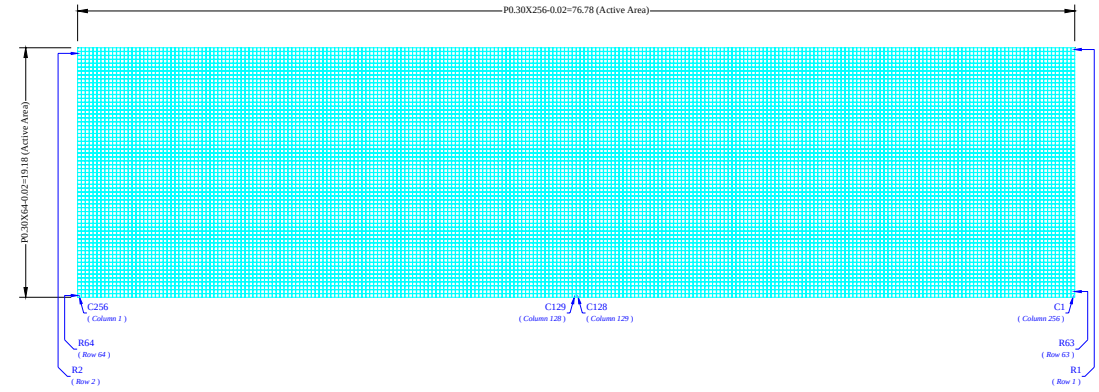
1.1 Display Specifications

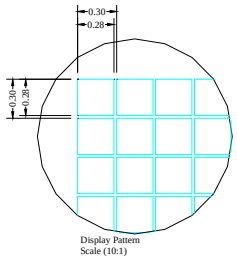
1) Display Mode: Passive Matrix
2) Display Color: Monochrome (Light Blue)
3) Drive Duty: 1/64 Duty

1.2 Mechanical Specifications

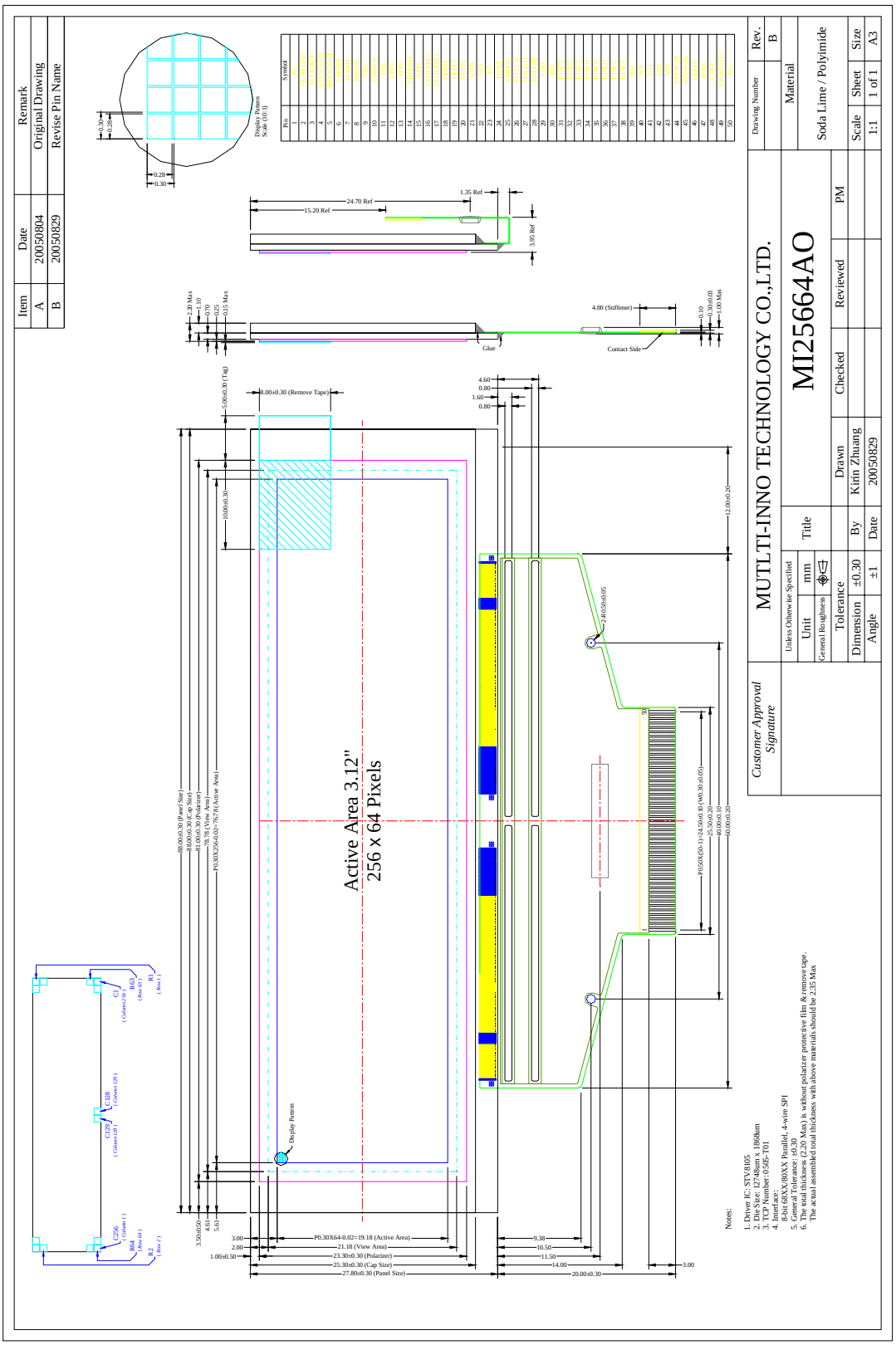
1) Outline Drawing: According to the annexed outline drawing number
2) Number of Pixels: 256 × 64
3) Panel Size: 88.00 × 27.80 × 2.20 (mm)
4) Active Area: 76.78 × 19.18 (mm)
5) Pixel Pitch: 0.30 × 0.30 (mm)
6) Pixel Size: 0.28 × 0.28 (mm)
7) Weight: 9.6 (g)

1.3 Active Area & Pixel Construction





1.4 Mechanical Drawing



1.5 Pin Definition

Pin Number	Symbol	I/O	Function
Power Supply			
21, 29	VDD	I	*Power Supply for Logic Circuit* These are the voltage supply pins. They must be connected to external source.
11, 22, 43	VSS	I	*Ground of OEL System* These are the ground pins. They also act as the reference for the logic pins. They must be connected to external ground.
15 13	VPP1 VPP2	I	*Power Supply for Odd (1) & Even (2) Column Driver* These are the constant current supply pins. They are supplied externally.
49 2	VROWOFF1 VROWOFF2	I	*Power Supply for Odd (1) & Even (2) Row Driver* These are the constant voltage supply pins. When display is not active, the row output pins are pulled-up to the voltage supplied on the two pins. They are supplied externally.
12	VPRG	I	*Power Supply for Non-Volatile OTP Memory Programming* This is the NVM programming voltage supply pin. It is supplied externally.
Driver			
17 16	VCOLPRE1 VCOLPRE2	I	*Power Supply for Odd (1) & Even (2) Column Pre-Charge* These are the constant voltage supply pins. They are supplied externally.
20 19	VREF1 VREF2	I/O	*Reference Voltage* These are the current reference pins. It is possible to set two different reference current values for the odd (1) and even (2) outputs by connecting two different resistor values. With input CMODE, it is also to use only the reference current established on pin VREF1. These are supplied externally.
DC/DC Converter			
9	VDC	I	*Power Supply for Gate Drive Output Buffer* This is the power supply pin for the internal buffer of the DC/DC voltage converter. It must be floated when the converter is not used.
10	VDRIVE	O	*Gate Drive Signal for External Switching FET* This output pin drives the gate of external power FET.
6	VSENSE	I	*Feedback Signal* This pin is the feedback signal for voltage regulation loop. It is used to adjust the booster output voltage level (VPP). In case of VSENSE feedback disconnection the Driver is switched off.
14	VHSENSE	I	*VPP Sense Input* This pin is the feedback signal for voltage regulation loop. It is used to adjust the booster output voltage level (VPP). In case of VHSENSE feedback disconnection, VPP voltage rises up to the value fixed by the external resistor divider.
8	ISENSE	I	*Over Current Sense Signal for External Switching FET* This pin is the feedback signal for current sense. It is used for over current protection on the external FET.

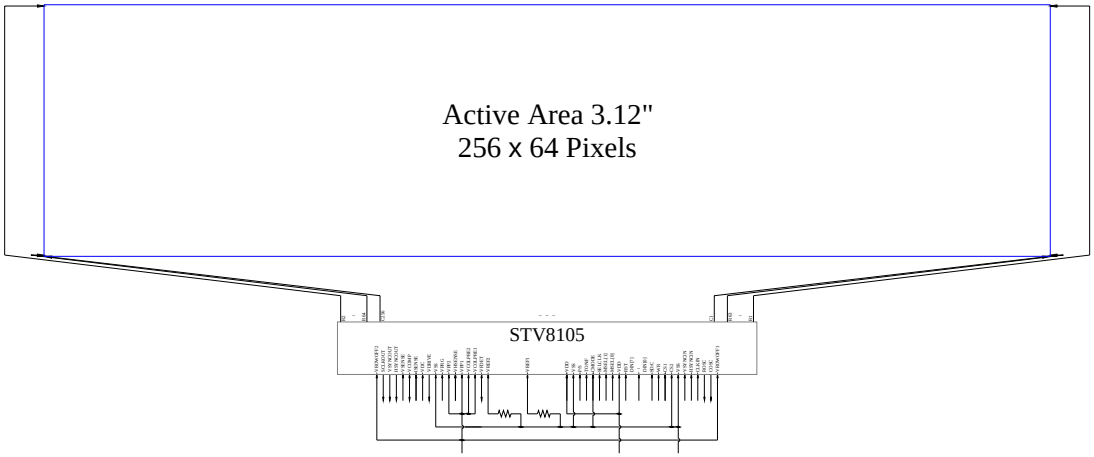
1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
DC/DC Converter (Continued)			
18	VFDET	I/O	*Pin for VF Detection* This pin is the detection of voltage difference between C1 and C256.
7	VCOMP	I/O	*Compensation Pin* The output of the amplifier VCOMP is externally available for compensation. It is necessary when the DC/DC converter works in PWM constant frequency mode. PFM constant t_{on} mode does not need a compensation network.
External IC Control			
44 4 45 5	VSYNCIN VSYNCOUT HSYNCIN HSYNCOUT	I O I O	*Vertical/Horizontal SYNC Input/Output* The "VSYNC" and "HSYNC" pins, both inputs and outputs, are connected for synchronous operation. These should be left open individually.
3	SCLKOUT	O	*System Clock Output* This pin is outputted to slave device and/or the specified row driver. It should be left open individually.
Clock			
46	CLKIN	I	*External System Clock Source* This pin is activated for the external RC/Crystal connection or Clock input.
47	ROSC	O	*External System Clock Source* This pin is activated for the external RC oscillator or Crystal oscillation. A resistor would be connected.
48	COSC	O	*External System Clock Source* This pin is activated for the external RC oscillator. A capacitor would be connected.
Configuration			
28	MSEL[0]	I	*Master/Slave Select* This pin is the Master/Slave selection input. The function is synchronous operation, which is the direction of the anode. This pin must be pulled high to enable the chip function as master.
27	MSEL[1]	I	*Primary/Secondary Select* This pin is the Primary/Secondary selection input. The function is synchronous operation, which is the direction of the cathode. This pin must be pulled high to enable the chip function as primary.
26	SELCLK	I	*Internal/External System Clock Source Select* This pin is internal clock enable. When this pin is pulled high, an internal oscillation stable circuit is used. The internal clock will be disabled when it is pulled low, an external clock source must be connected for normal operation.

1.5 Pin Definition (Continued)

Pin Number	Symbol	I/O	Function
Configuration (Continued)			
24	TON/F	I	*DC/DC Converter Mode Select* This pin is the control schemes selection input of the embedded booster circuit. The DC/DC converter works in PFM constant t_{on} mode while it is connected to VDD. The DC/DC converter works in PWM constant frequency mode while it is connected to ground.
25	CMODE	I	*Color Mode Select* This pin is the display colors selection input. It corresponds to "Two" color display panel. A setup of another output current value is possible for an odd number pin and the even number pins of each with two reference current.
Interface			
23	P/S	I	*Communicating Protocol Select* This pin is MCU interface selection input. The parallel interface is active when P/S is high; the serial interface activates when P/S is low.
30	RST	I	*Power Reset for Controller and Driver* This pin is reset signal input. When the pin is low, initialization of the chip is executed.
41 42	CS1 CS2	I	*Chip Select* The two pins are the chip select input. The CS1 is activated for Primary/Secondary Master devices. The CS2 is activated for Primary/Secondary Slave devices.
40	WR	I	*Write Pulse* This pin is MCU interface input. Data write operation is initiated when this pin is pulled low and the chip is selected.
39	SD/C	I	*Data/Command Control* This pin is Data/Command control pin. When the pin is pulled high, the data at DIN[7]~DIN[0] is treated as display data. When the pin is pulled low, the data at DIN[7]~DIN[0] will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.
31~38	DIN[7]~DIN[0]	I	*Host Data Input Bus* These pins are 8-bit parallel bus to be connected to the microprocessor's data bus. When serial mode is selected, DIN[7] will be the serial data input (SIN) and DIN[6] will be the serial clock input (SCLI).
Reserve			
1, 50	N.C.	-	*Reserved Pin (Supporting Pin)* The supporting pins can reduce the influences from stresses on the function pins.

1.6 Block Diagram



MCU Interface Selection: P/S
Pins connected to MCU interface:
RST, DIN[7]~DIN[0], SD/C, WR, and CS1

2. Absolute Maximum Ratings

2.1 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Notes
Supply Voltage	V_{DD}	-0.3	4.6	V	1, 2
DC/DC Supply Voltage	V_{DC}	-0.3	12	V	1, 2
Driver Supply Voltage	V_{PP}	-0.3	27	V	1, 2
Program Voltage	V_{PRG}	-0.3	20	V	1, 2
Operating Temperature	T_{OP}	-20	70	°C	-
Storage Temperature	T_{STG}	-30	80	°C	-

Note 1: All the above voltages are on the basis of "GND = 0V".

Note 2: When this module is used beyond the above absolute maximum ratings, permanent breakage of the module may occur. Also, for normal operations, it is desirable to use this module under the conditions according to Section 3. "Electrical Characteristics". If this module is used beyond these conditions, malfunctioning of the module can occur and the reliability of the module may deteriorate.

2.2 Regarding the Gradation

Although this module possesses the gradation function, respective gradation levels will vary depending on the production conditions etc. Also, the temperature range where the gradation function can be guaranteed will be -10°C~60°C.

3. Electrical Characteristics

3.1 DC Characteristics

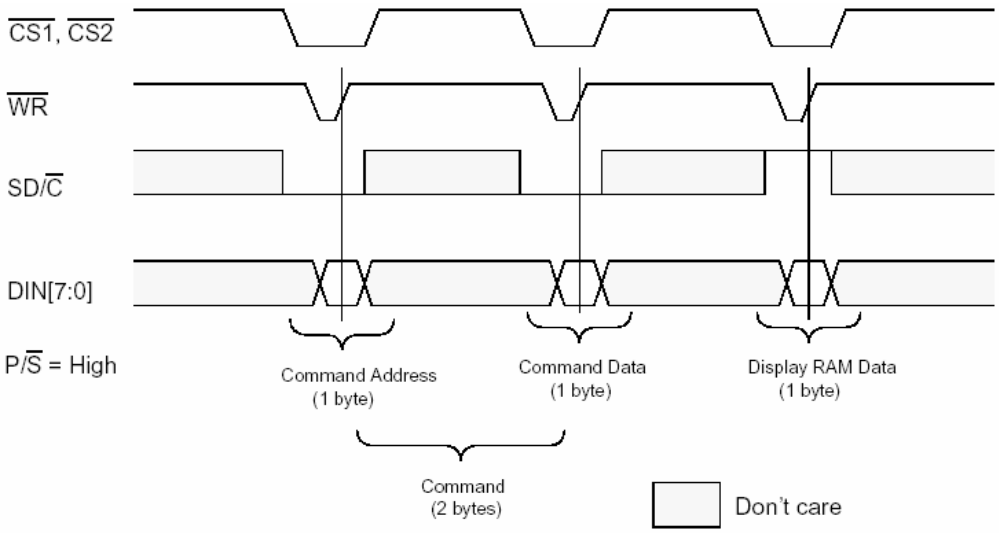
Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		3.0	3.3	3.6	V
DC/DC Supply Voltage	V_{DC}		3.0	5.0	10.0	V
Driver Supply Voltage	V_{PP}		-	14	-	V
Program Voltage	V_{PRG}		14	-	18	V
High Level Input	V_{IH}	Logic	$0.8\times V_{DD}$	-	-	V
Low Level Input	V_{IL}	Logic	-	-	$0.2\times V_{DD}$	V
High Level Output	V_{OH}	Sinking Current > -1mA	$0.8\times V_{DD}$	-	-	V
Low Level Output	V_{OL}	Sourcing Current < 1mA	-	-	$0.2\times V_{DD}$	V

3.2 AC Characteristics

3.2.1 Parallel Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
T_{ah}	Address Hold Time	10	-	ns
T_{aw}	Address Setup Time	0	-	ns
T_{cyc}	System Cycle Time	200	-	ns
T_{ds}	Data Setup Time	60	-	ns
T_{dh}	Data Hold Time	10	-	ns
T_{cclw}	Write Pulse Width	60	-	ns

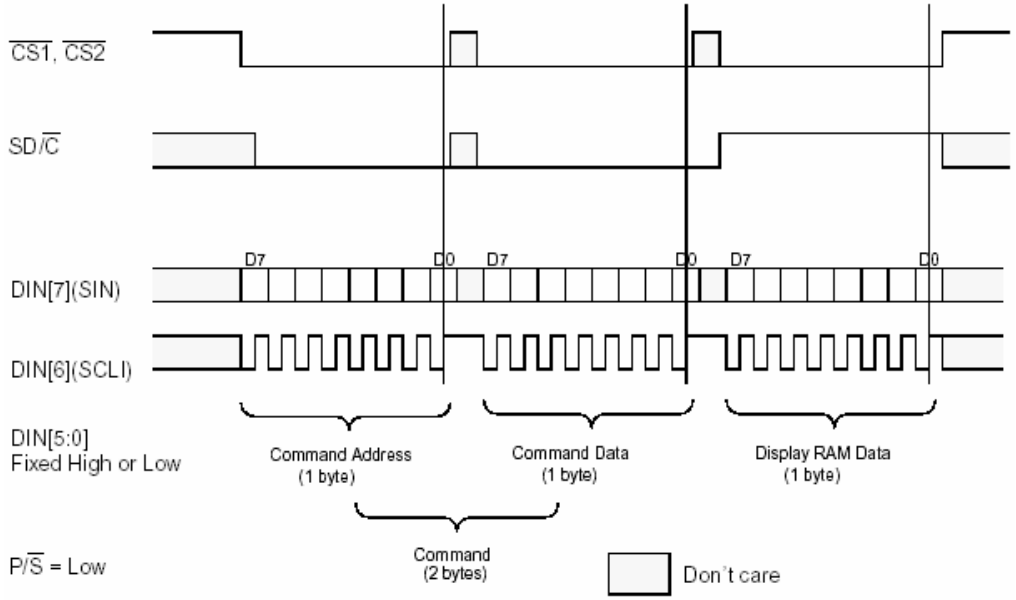
* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.2.2 Serial Interface Timing Characteristics:

Symbol	Description	Min	Max	Unit
T_{scyc}	Serial Clock Cycle Time	200	-	ns
T_{sas}	Address Setup Time	20	-	ns
T_{sah}	Address Hold Time	20	-	ns
T_{css}	Chip Select Setup Time	20	-	ns
T_{csh}	Chip Select Hold Time	20	-	ns
T_{sds}	Data Setup Time	20	-	ns
T_{sdh}	Data Hold Time	20	-	ns
T_{slw}	Pulse Width (Low)	90	-	ns
T_{shw}	Pulse Width (High)	90	-	ns

* All the timings should be based on 30% and 70% of V_{DD}-GND.



3.3 Optics & Electrical Characteristics

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Brightness	L_{br}	With Polarizer	60	80	-	cd/m^2
C.I.E. (Blue)	(x) (y)	Without Polarizer	0.12 0.28	0.16 0.32	0.20 0.36	
Dark Room Contrast	CR		-	>1:100	-	
View Angle			>160	-	-	degree

Note 3: Optical measurement taken at 1/64 duty, 100Hz Frame Rate,
7Fh Luminance Adjustment Setting.

3.4 General Electrical Specification

Characteristics	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		3.0	3.3	3.6	V
DC/DC Supply Voltage	V_{DC}		3.0	5.0	10.0	V
Driver Supply Voltage	V_{PP}		13	14	15	V
Program Voltage	V_{PRG}		14	-	18	V
Operating Current for V_{DD}	I_{DD}	Note 4	-	0.6	1.0	mA
		Note 5	-	0.6	1.0	mA
Operating Current for V_{PP}	I_{PP}	Note 4	-	20	25	mA
		Note 5	-	32	40	mA
Sleep Mode Current for V_{DD}	$I_{DD, SLEEP}$		-	40	70	μA
Sleep Mode Current for V_{PP}	$I_{PP, SLEEP}$		-	<1	-	μA

Note 4: V_{DD} = 3.3V, V_{PP} = 14V, Frame Rate = 100Hz,
Luminance Adjustment Setting = 7Fh, 50% Display Area Turn on.
Note 5: V_{DD} = 3.3V, V_{PP} = 14V, Frame Rate = 100Hz,
Luminance Adjustment Setting = 7Fh, 100% Display Area Turn on.

4. Functional Specification

4.1. Commands

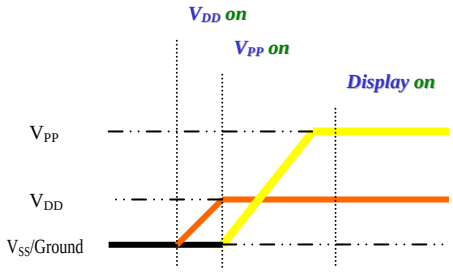
Refer to the Technical Manual for the STV8105

4.2 Power down and Power up Sequence

To protect OEL panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

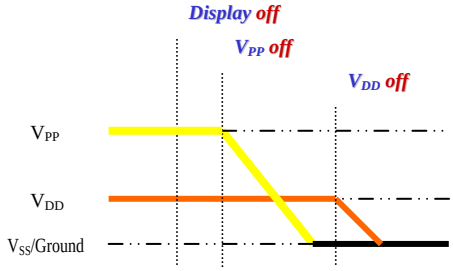
4.2.1 Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Clear Screen
4. Power up V_{PP}
5. Delay 100ms
   (when V_{DD} is stable)
6. Send Display on command



4.2.2 Power down Sequence:

1. Send Display off command
2. Power down V_{PP}
3. Delay 100ms
   (when V_{PP} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



4.3 Reset Circuit

At the time of RST signal input…

Oscillator:	Off
DC/DC Converter:	Off
Column & Row Driver:	V_{SS}
All Registers:	Default Value

At the time of RST signal release or software reset completion (200ns maximum after F2h command sending)…

Oscillator:	On
DC/DC Converter:	Off (Waiting for a Command)
Column & Row Driver:	V_{SS} (Waiting for a Command)
All Registers:	Default Value (Waiting for a Command)

5. *Reliability*

5.1 Contents of Reliability Tests

Item	Conditions	Criteria
High Temperature Operation	85°C, 500 hrs	The brightness should be greater than 50% of the initial brightness. The operational functions work.
Low Temperature Operation	-30°C, 500 hrs	
High Temperature Storage	90°C, 500 hrs	
Low Temperature Storage	-40°C, 500 hrs	
High Temperature/Humidity Operation	60°C, 90% RH, 500 hrs	
Thermal Shock	-40°C ⇔ 85°C, 100 cycles **60** mins dwell	

* The samples used for the above tests do not include polarizer.
* No moisture condensation is observed during tests.
* All operation tests are conducted in all display on pattern.

5.2 Lifetime

End of lifetime is specified as 50% of initial brightness.
An estimated operating lifetime of more than 8,000 hrs at room temperature is approached by **high temperature operating test**.

5.3 Failure Check Standard

After the completion of the described reliability test, the samples were left at room temperature for 2 hrs prior to conducting the failure test at 23±5°C; 55±15% RH.

6. Outgoing Quality Control Specifications

6.1 Environment Required

Customer's test & measurement are required to be conducted under the following conditions:

Temperature:	23 ± 5°C
Humidity:	55 ± 15 %RH
Fluorescent Lamp:	30W
Distance between the Panel & Lamp:	≥ 50 cm
Distance between the Panel & Eyes of the Inspector:	≥ 30 cm

Finger glove (or finger cover) must be worn by the inspector.
Inspection table or jig must be anti-electrostatic.

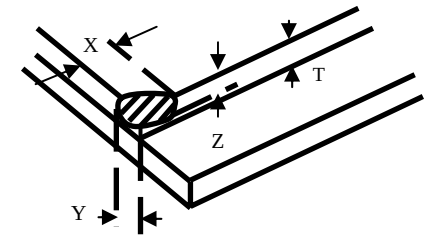
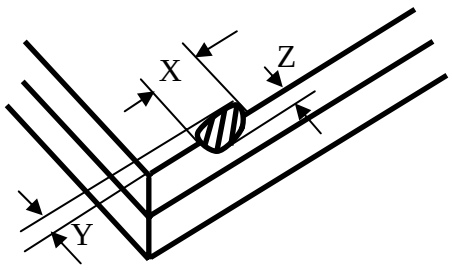
6.2 Sampling Plan

Level II, Normal Inspection, Single Sampling, MIL-STD-105E

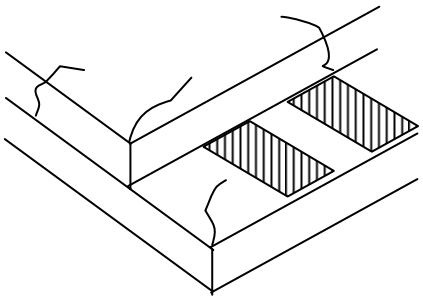
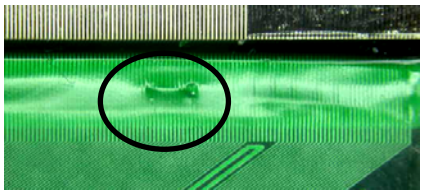
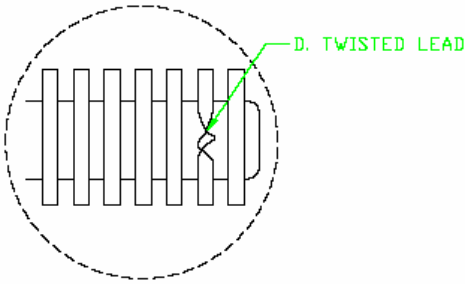
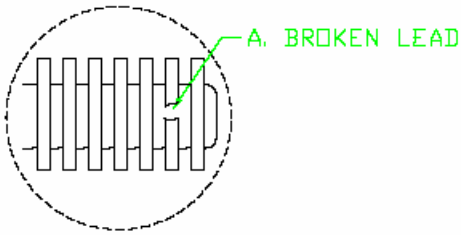
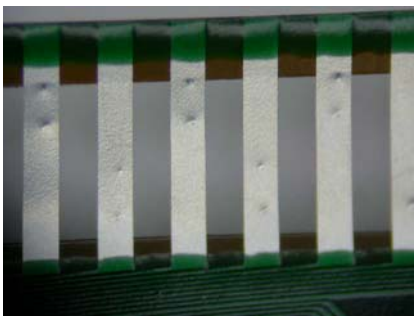
6.3 Criteria & Acceptable Quality Level

Partition	AQL	Definition
Major	0.65	Defects in Pattern Check (Display On)
Minor	1.0	Defects in Cosmetic Check (Display Off)

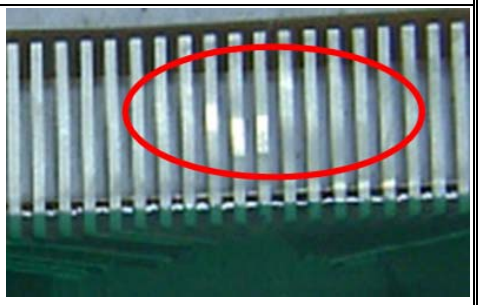
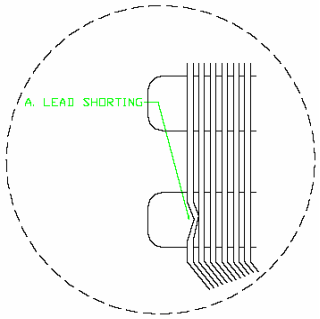
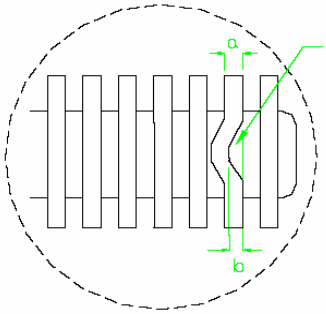
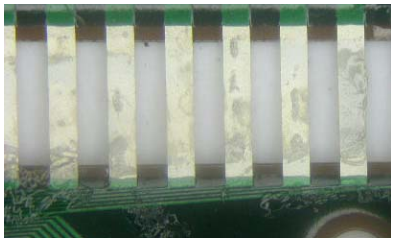
6.3.1 Cosmetic Check (Display Off) in Non-Active Area

Check Item	Classification	Criteria
Panel General Chipping	Minor	X > 6 mm (Along with Edge) Y > 1 mm (Perpendicular to edge) Z ≤ T  

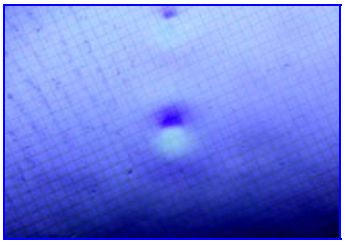
6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Panel Crack	Minor	Any crack is not allowable. 
Cupper Exposed (Even Pin or Film)	Minor	Not Allowable by Naked Eye Inspection
Film or Trace Damage	Minor	
Terminal Lead Twist	Minor	Not Allowable 
Terminal Lead Broken	Minor	Not Allowable 
Terminal Lead Probe Mark	Acceptable	

6.3.1 Cosmetic Check (Display Off) in Non-Active Area (Continued)

Check Item	Classification	Criteria
Terminal Lead Crooked	Acceptable	
Terminal Lead Bent (Not Twist or Broken)	Minor	NG if any bent lead cause lead shorting. 
	Minor	NG for horizontally bent lead more than 50% of its width. 
Glue or Contamination on Pin (Couldn't Be Removed)	Minor	
Ink Marking on Back Side of panel (Exclude on Film)	Acceptable	Ignore for Any

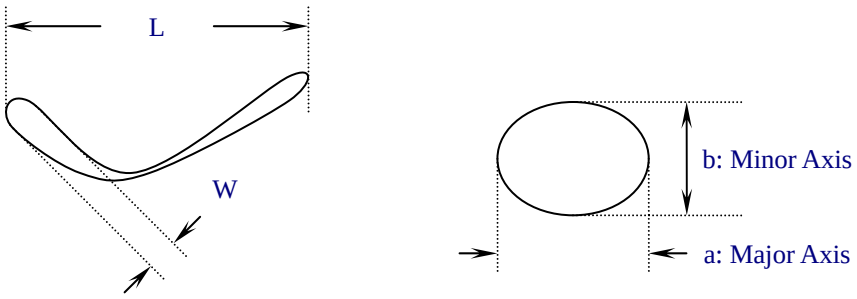
6.3.2 Cosmetic Check (display off) in Active Area

Check Item	Classification	Criteria
Any Dirt & Scratch on Polarizer's Protective Film	Acceptable	Ignore for not Affect the Polarizer
Scratches, Fiber, Line-Shape Defect ** (On Polarizer)	Minor	W ≤ 0.05 Ignore W ≤ 0.1, L ≤ 2 n ≤ 1 2 < L n = 0
Dirt, Black Spot, Foreign Material, ** (On Polarizer)	Minor	Φ ≤ 0.1 Ignore 0.1 < Φ ≤ 0.25 n ≤ 1 0.25 < Φ n = 0
Dent, Bubbles, White spot (Any Transparent Spot on Polarizer)	Minor	Φ ≤ 0.5 ➔ Ignore if no Influence on Display 0.5 < Φ n = 0 
Fingerprint, Flow Mark (On Polarizer)	Minor	Not Allowable

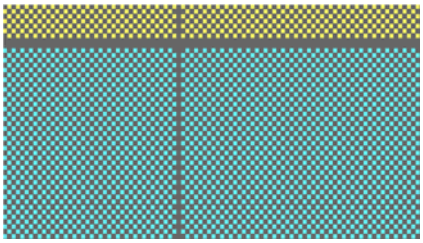
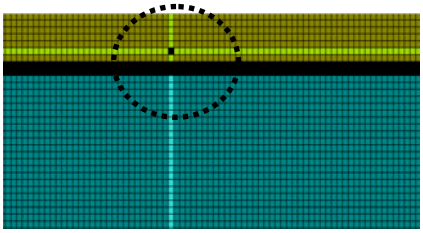
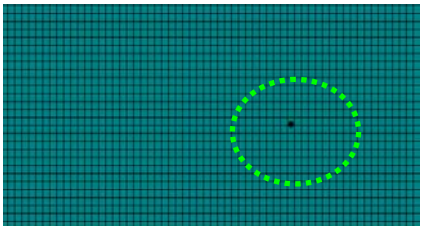
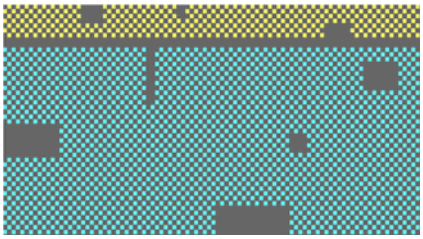
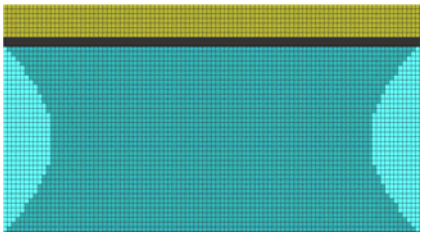
* The protective film shall not be tear off when cosmetic check.

** Distance between any 2 defects should over 10mm.

*** Definition of W & L & Φ (Unit: mm): Φ = (a + b) / 2



6.3.3 Pattern Check (Display On) in Active Area

Check Item	Classification	Criteria
No Display	Major	
Flicker	Major	Not Allowable
Missing Line	Major	
Pixel Short	Major	
Darker Pixel	Major	
Wrong Display	Major	
Un-uniform	Major	

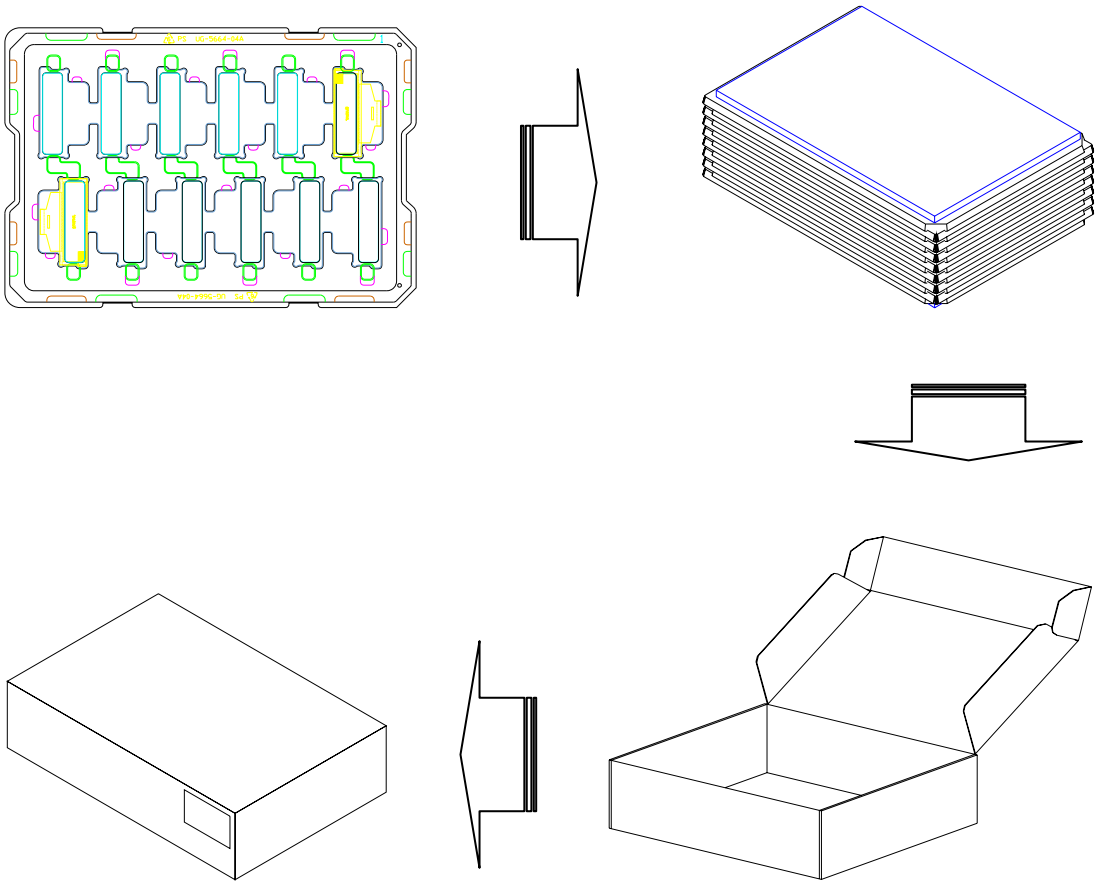
7. Package Specifications

7.1 Inner Carton Box

Each OEL display module will be placed on the antistatic tray and up to 180 units at the maximum will be packaged into the inner carton box. A label indicating the flowing contents will be applied to the surface of the inner carton box.

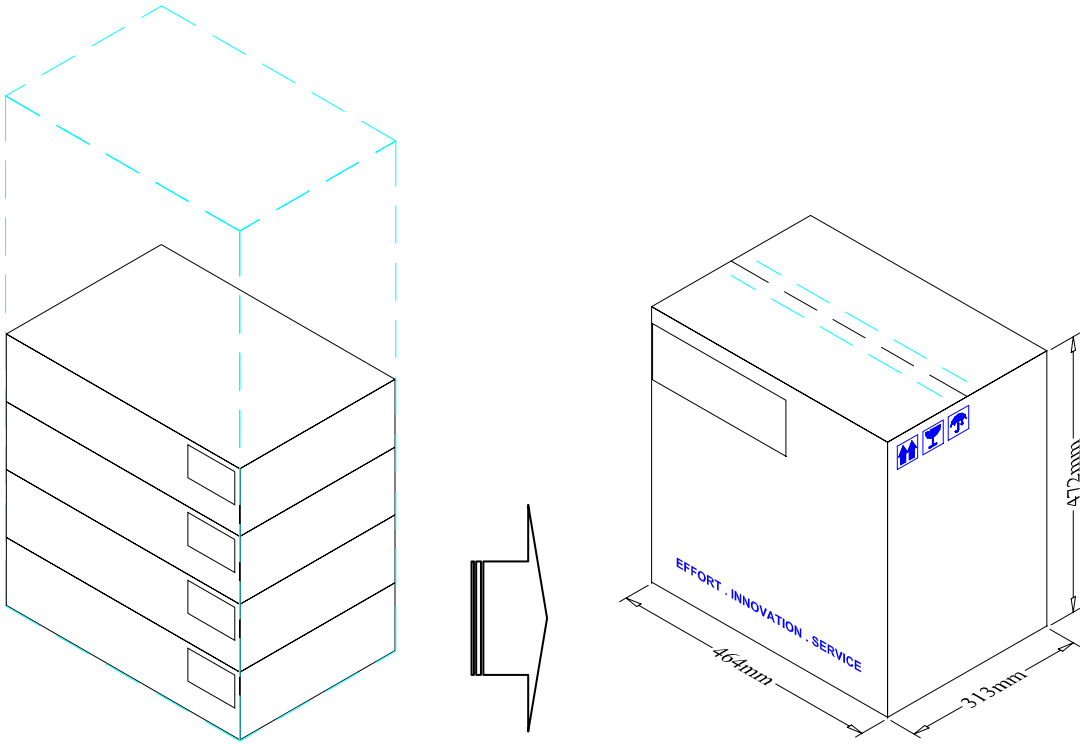
Product Number: MI25664AO	
Quantity 180 pieces	**Lot** XXXXXXXX
Customer Product Number: XXXXXXXXXXX	
QC Check :	**Date:** 2005.8.30

Contents of the label indication



7.2 Master Carton Box

The Master Carton Box is the unit package to deliver to each customer. The Master Carton Box contains 4 inner carton boxes.



8. Precautions When Using These OEL Display Modules

8.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.
3) If pressure is applied to the display surface or its neighborhood of the OEL display module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the OEL display module is soft and easily scratched. Please be careful when handling the OEL display module.
5) When the surface of the polarizer of the OEL display module has soil, clean the surface. It takes advantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent

   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.

   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) When installing the OEL display module, be careful not to apply twisting stress or deflection stress to the OEL display module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.
7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the OEL display module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing OEL display modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling OEL display modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the OEL display module. Be careful since static electricity may be generated when exfoliating the protective film.
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the OEL display module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

8.2 Storage Precautions

1) When storing OEL display modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Mutli-Inno Technology Inc.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the OEL display module, when the OEL display module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

8.3 Designing Precautions

1) The absolute maximum ratings are the ratings which cannot be exceeded for OEL display module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
4) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
5) As for EMI, take necessary measures on the equipment side basically.
6) When fastening the OEL display module, fasten the external plastic housing section.
7) If power supply to the OEL display module is forcibly shut down by such errors as taking out the main battery while the OEL display panel is in operation, we cannot guarantee the quality of this OEL display module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows: STV 8105
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

8.4 Precautions when disposing of the OEL display modules

1) Request the qualified companies to handle industrial wastes when disposing of the OEL display modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

8.5 Other Precautions

1) When an OEL display module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.

Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module.

2) To protect OEL display modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the OEL display modules.
   * Pins and electrodes
   * Pattern layouts such as the TCP
3) With this OEL display module, the OEL driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this OEL driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the OEL driver may be shielded from light in actual usage.
   * Design the product and installation method so that the OEL driver may be shielded from light during the inspection processes.
4) Although this OEL display module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed. It therefore is necessary to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.