MULTI-INNO TECHNOLOGY CO., LTD.

OLED MODULE SPECIFICATION

Model : MI12864PO

Revision	1.1
Engineering	
Date	
Our Reference	

CONTENT

REVISION RECORD

REV.	REVISION DESCRIPTION	REV.DATE	PAGE
1.0	First Issue	2008-03-17	All
1.1	Modify PIN order of section 4 Mechanical Drawing and section 13 Contact us	2008-08-05	P5，P21

1 Overview

MI12864PO is an OLED monochrome 128×64 dot matrix display module. The characteristics of this display module are high brightness, self-emission, high contrast ratio, slim/thin outline, wide viewing angle, wide temperature range, and low power consumption.

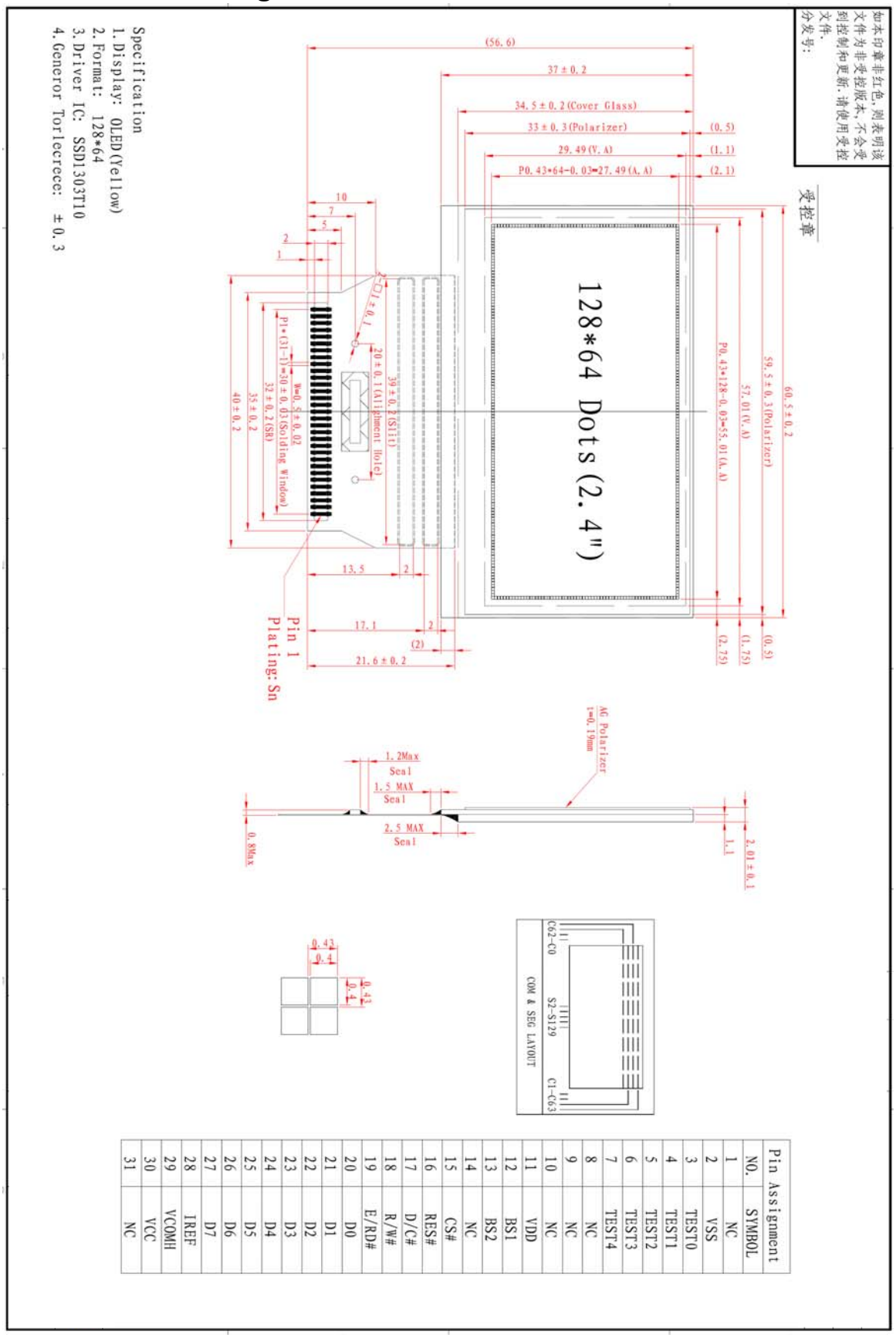
2 Features

- High contrast ratio
- Color: Yellow
- 128×64pixels
- Wide viewing angle
- Wide range of operating temperature
- low power consumption
- 8-bit 8080-Databus or 8-bit 6800-series parallel interface or series peripheral interface or I^2C interface.
- Display data is stored in Display Data RAM from MPU
- Built-in SSD1303 standard OLED controller

3 Mechanical Data and Part Number

NO.	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128(W) x 64(rows)	-
2	Dot Size	0.4(W) x 0.4 (H)	mm
3	Dot Pitch	0.43 (W) x 0.43 (H)	mm
4	Aperture Rate	86	%
5	Active Area	55.01 (W) x 27.49 (H)	m2
7	Module Size	60.5 (W) x 56.6 (H) x 2.01(D)	mm
8	Polarizer	with	
9	Duty	1/64	

4 Mechanical Drawing

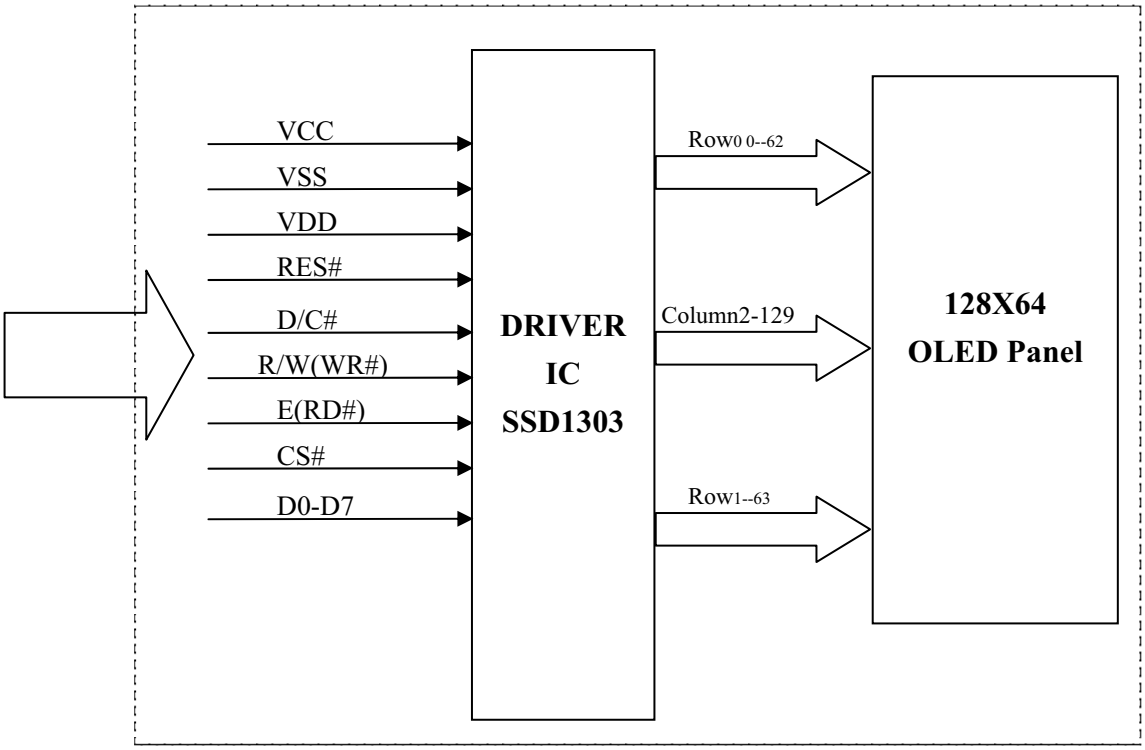


5 Module Interface

<table>
<tr><th>PIN NO</th><th>PIN NAME</th><th>DESCRIPTION</th></tr>
<tr><td>1</td><td>NC</td><td>No Connection</td></tr>
<tr><td>2</td><td>VSS</td><td>Ground</td></tr>
<tr><td>3</td><td>Test0</td><td rowspan="5">Reserved pin; No connection and left float.</td></tr>
<tr><td>4</td><td>Test1</td></tr>
<tr><td>5</td><td>Test2</td></tr>
<tr><td>6</td><td>Test3</td></tr>
<tr><td>7</td><td>Test4</td></tr>
<tr><td>8</td><td>NC</td><td rowspan="3">No connection</td></tr>
<tr><td>9</td><td>NC</td></tr>
<tr><td>10</td><td>NC</td></tr>
<tr><td>11</td><td>VDD</td><td>Power supply for interface logic level. It should be match with MCU interface voltage level. VDDIO must always be equal or lower than VDD.</td></tr>
<tr><td>12</td><td>BS1</td><td rowspan="2">These are MCU interface input selection pins. See the following table for selecting different interfaces:
<table>
<tr><th>Pin Name</th><th>I2C Inter face</th><th>6800-parallel Interface</th><th>8080-parallel interface</th><th>Serial interface</th></tr>
<tr><td>BS1</td><td>1</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>BS2</td><td>0</td><td>1</td><td>1</td><td>0</td></tr>
</table></td></tr>
<tr><td>13</td><td>BS2</td></tr>
<tr><td>14</td><td>NC</td><td>No Connection</td></tr>
<tr><td>15</td><td>CS#</td><td>Chip Select, active low</td></tr>
<tr><td>16</td><td>RES#</td><td>Reset, active low</td></tr>
<tr><td>17</td><td>D/C#</td><td>Data/Command Select. This is the Data/Command control pin. When it is pulled HIGH, the input at D7-D0 is treated as display data. When it is pulled LOW, the input at D7-D0 is transferred to the command registers. For detail relationship to MCU interface signals, please refer to the Timing Characteristics Diagrams.</td></tr>
<tr><td>18</td><td>R/W(WR#)</td><td>This is a MCU interface input pin. When 6800-series Parallel Interface mode is selected, this pin is used as Read/Write (R/W) selection input. Pull this pin to HIGH for read mode and pull it to LOW for write mode.
When 8080-series Parallel Interface mode is selected, this pin is used as Write (WR#) selection input. Pull this pin to LOW for write mode. Data write operation is initiated when this pin is pulled LOW and the CS# is pulled LOW.</td></tr>
<tr><td>19</td><td>E(RD#)</td><td>This is a MCU interface input pin. When 6800-series Parallel Interface is selected, this pin is used as Enable (E) signal. Read/Write operation is initiated when this pin is pulled HIGH and the CS# pin is pulled LOW. When 8080-series Parallel Interface is selected, this pin is used to receive the Read Data (RD#)signal. Data read operation is initiated when this pin is pulled LOW and CS# pin is pulled LOW.</td></tr>
<tr><td>20-27</td><td>D0-D7</td><td>These are 8-bit bi-directional data bus to be connected to the microprocessor’s data bus. When serial interface mode is selected, D1 will be the serial data input, SDIN, and D0 will be the serial clock input, SCLK.</td></tr>
<tr><td>28</td><td>IREF</td><td>This is a segment current reference pin. A resistor should be connected between this pin and VSS. Set thecurrent at 10uA.</td></tr>
<tr><td>29</td><td>VCOMH</td><td>This is an input pin for the voltage output high level for COM signals. A capacitor should be connected between this pin and VSS.</td></tr>
<tr><td>30</td><td>VCC</td><td>OLED drive voltage, It should be supplied externally.</td></tr>
<tr><td>31</td><td>NC</td><td>No Connection</td></tr>
</table>

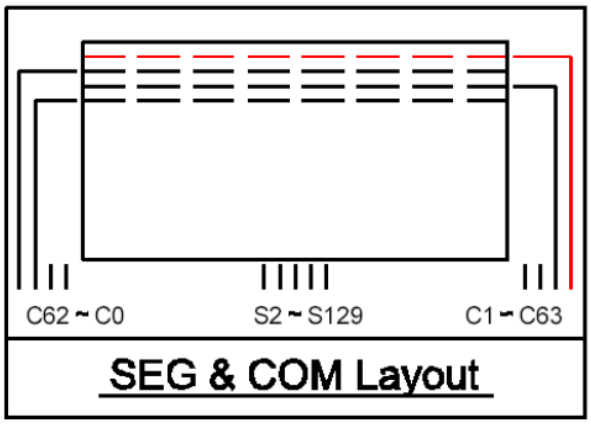
6 Function Block Diagram

6.1 Function Block Diagram



NOTE: Some pins omitted

6.2 PANEL LAYOUT DIAGRAM



7 Absolute Maximum ratings

ITEM	Symbol	MIN	MAX	Unit	Conditions	Remark
Logic supply voltage	V_{DD}	-0.3	+3.5	V	Ta = 25 °C	IC maximum rating
OLED Operating voltage	V_{CC}	8	+16	V	Ta = 25 °C	IC maximum rating
Operating Temp.	Top	-40	+80	℃		
Storage Temp	Tstg	-45	+85	℃		
Life Time		40,000			100 cd/m^2, 50% checkerboard	Note(1)
Life Time		50,000			80 cd/m^2, 50% checkerboard	Note(2)
Life Time		66,000			60 cd/m^2, 50% checkerboard	Note(3)

Note:

(A) Under VCC = 13V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 100 cd/m^2:

- Contrast setting : 0XC5
- Frame rate : 105Hz
- Duty setting : 1/64

(2) Setting of 80 cd/m^2:

- Contrast setting : 0x8F
- Frame rate : 105Hz
- Duty setting : 1/64

(3) Setting of cd/m^2:

- Contrast setting : 0x4C
- Frame rate : 105Hz
- Duty setting : 1/4

8 Electrical Characteristics

8.1 DC Electrical Characteristics

ITEM	Symbol	Test condition	MIN	TYPE	MAX	Unit
Logic Supply Voltage	V_{DD}	Ta=-20℃ to +70℃	2.4	2.7	3.5	V
OLED Driver Supply Voltage	V_{CC}	Ta=-20℃ to +70℃	12.5	13	13.5	V
Operating Current for V_{DD}	I_{DD}	Contrast=FF	-	190	300	μA
Operating Current for V_{PP}	I_{CC}	Contrast=FF	-	550	1000	μA
High-level Input Voltage	V_{IH}		0.8*V_{DD1}	-	-	V
Low-level Iinput Voltage	V_{IL}		0	-	0.2*V_{DD1}	V
High-level Output Voltage	V_{OH}	-	0.9*V_{DD1}	-	-	V
High-level Output Voltage	V_{OL}	-	0	-	0.1*V_{DD1}	V

Note 1: V_{DD} = 2.7V, V_{CC} =13V, Frame Rate = 105Hz, No panel attached.

Note 2: The V_{CC} input must keep in a stable value; ripple and noise are not allowed.

8.2 Electro-optical Characteristics

Item	Symbol	Test condition	MIN	TYPE	MAX	Unit
Normal mode Power consumption		All pixels on(1)			400	mW
Standby mode Power consumption		Standby mode 10% pixels on(2)			45	mW
Brightness	L_{br}	With polarizer	60	80	-	cd/m^2
C.I.E(Yellow)	(x)	x,y(CIE1931)	0.43	0.47	0.51	
	(y)		0.45	0.49	0.53	
Dark room contrast	CR		2000:1	-	-	
View angle			160			degree

(1) Normal mode condition

- Driving Voltage : 13V
- Contrast setting : 0x8F
- Frame rate : 105Hz
- Duty setting : 1/64

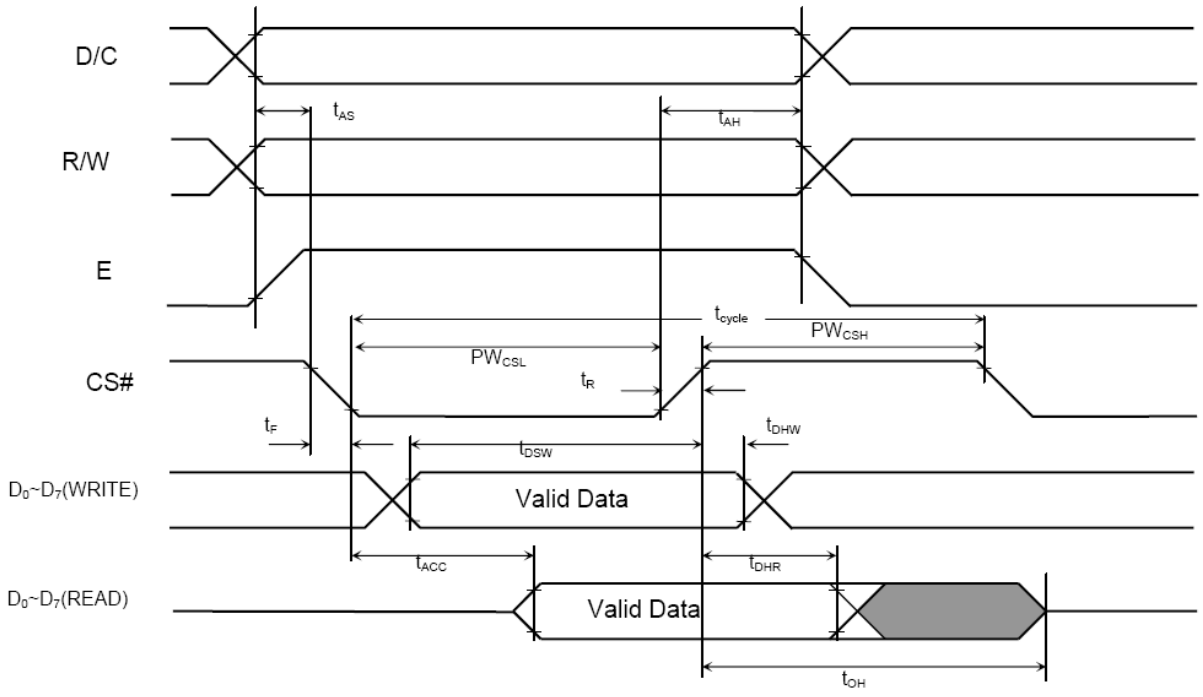
(2) Standby mode condition

- Driving Voltage : 13V
- Contrast setting : 0x00
- Frame rate : 105Hz
- Duty setting : 1/64

8.3 AC Electrical Characteristics

6800-Series MPU Parallel Interface Timing Characteristics (TA =25°C)

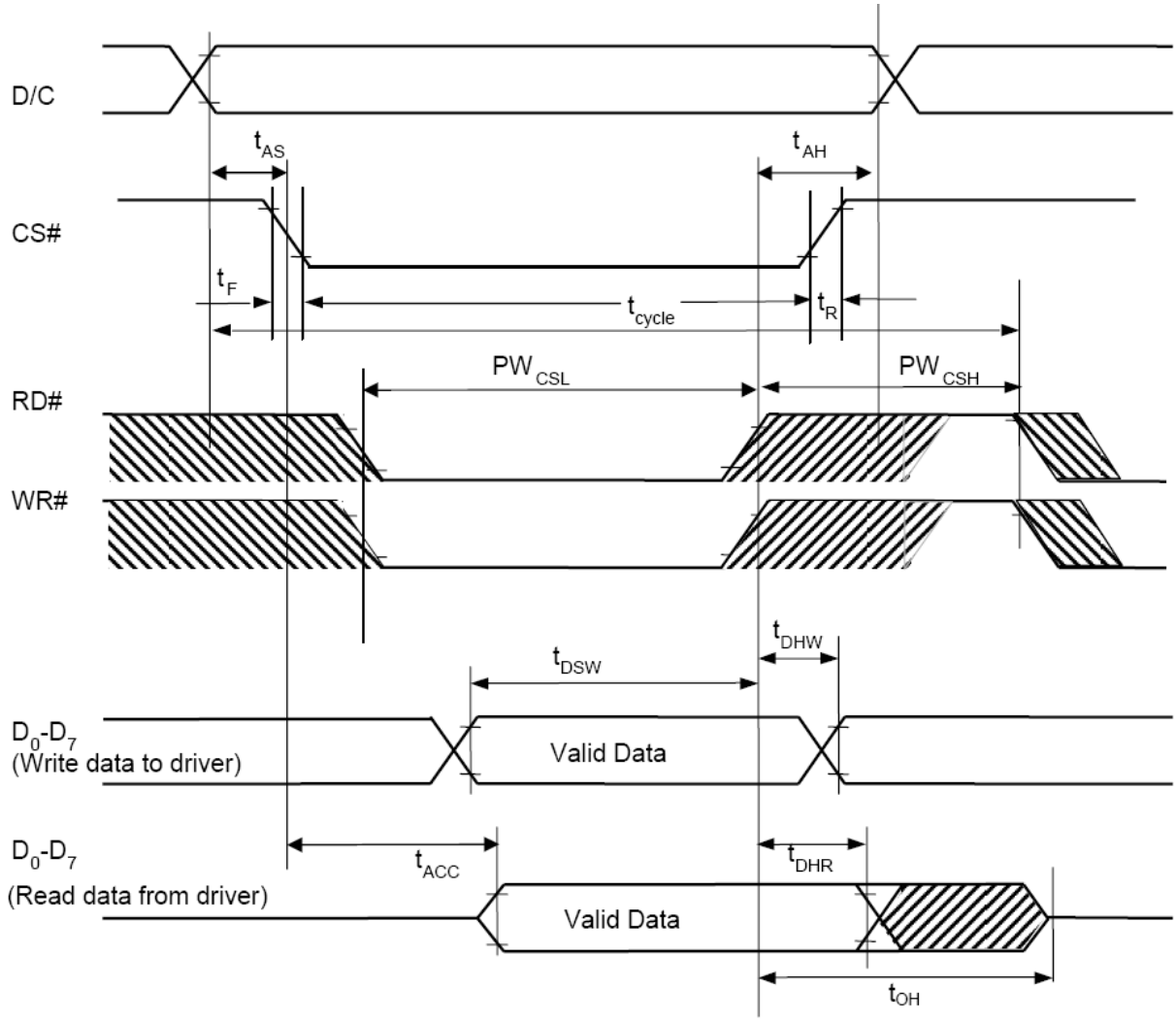
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	120 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



6800-series MPU parallel interface characteristics

8080-Series MPU Parallel Interface Timing Characteristics (TA =25°C)

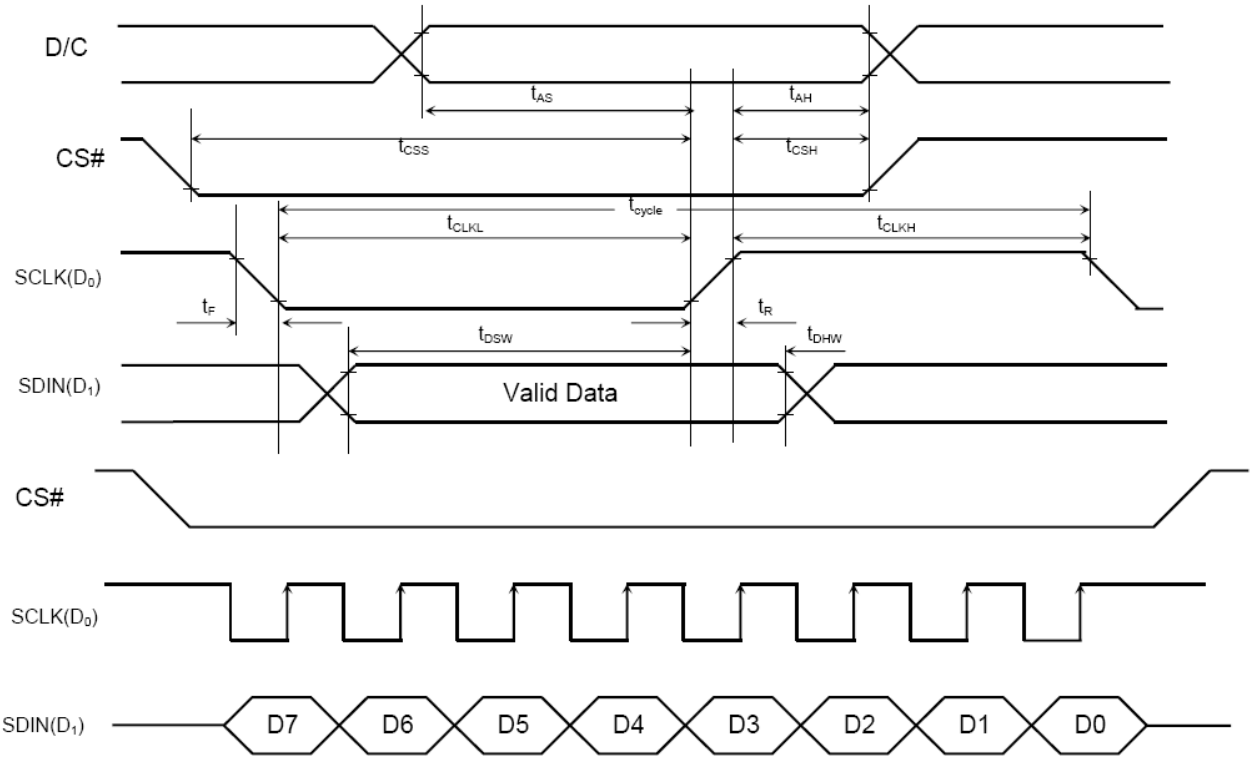
Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	7	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read) Chip Select Low Pulse Width (write)	150 60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read) Chip Select High Pulse Width (write)	60 60	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns



8080-series MPU parallel interface characteristics

Serial Interface Timing Characteristics (TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	100	-	-	ns
t_{DHW}	Write Data Hold Time	100	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	40	ns
t_F	Fall Time	-	-	40	ns

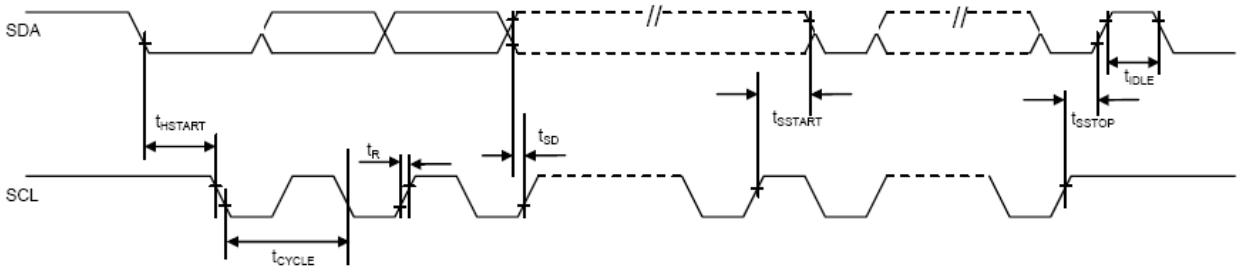


Serial interface characteristics

I²C Interface Timing Characteristics (TA = 25°C)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	2.5	-	-	us
t_{HSTART}	Start condition Hold Time	0.6	-	-	us
t_{SD}	Data Setup Time	100	-	-	ns
t_{SSTART}	Start condition Setup Time (Only relevant for a repeated Start condition)	0.6	-	-	us
t_{SSTOP}	Stop condition Setup Time	0.6	-	-	us
t_R	Rise Time for data and clock pin	-	-	300	ns
t_{IDLE}	Idle Time before a new transmission can start	1.3	-	-	us

I²C Interface Timing Characteristics



9 Display Control Instruction

Command table (D/C =0, R/W (WR#)=0, E (RD#)=1)

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	00~0F	0	0	0	0	X_3	X_2	X_1	X_0	Set Lower Column Address **	Set the lower nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after RESET.
0	10~1F	0	0	0	1	X_3	X_2	X_1	X_0	Set Higher Column Address **	Set the higher nibble of the column address register using $X_3X_2X_1X_0$ as data bits. The initial display line register is reset to 0000b after RESET.
0	26	0	0	1	0	0	1	1	0	Horizontal scroll setup	A[2:0] Set the number of column scroll per step
0	A[2:0]	*	*	*	*	*	A_2	A_1	A_0		Valid value: 001b, 010b, 011b, 100b
0	B[2:0]	*	*	*	*	*	B_2	B_1	B_0		B[2:0] Define start page address
0	C[1:0]	*	*	*	*	*	*	C_1	C_0		C[1:0] Set time interval between each scroll step in terms of frame frequency
0	D[2:0]	*	*	*	*	*	D_2	D_1	D_0		00b – 12 frame 01b – 64 frames 10b – 128 frames 11b – 256 frames D[2:0] Define end page address Set the value of D[2:0] larger or equal to B[2:0]
0	2F	0	0	1	0	1	1	1	1	Activate horizontal scroll	Start horizontal scrolling
0	2E	0	0	1	0	1	1	1	0	Deactivate horizontal scroll	Stop horizontal scrolling
0	40-7F	0	1	X_5	X_4	X_3	X_2	X_1	X_0	Set Display Start Line	Set display RAM display start line register from 0-63 using $X_5X_3X_2X_1X_0$. Display start line register is reset to 000000 during RESET
0	81	1	0	0	0	0	0	0	1	Set Contrast Control Register **	Double byte command to select 1 out of 256 contrast steps. Contrast increases as the value increases. (RESET = 80h)
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	82	1	0	0	0	0	0	1	0	Brightness for color banks	Double byte command to select 1 out of 256 brightness steps. Brightness increases as the value increases. (RESET = 80h)
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	91	1	0	0	1	0	0	0	1	Set Look Up Table (LUT)	Set current drive pulse width of Bank 0, Color A, B and C.
0	X[5:0]	*	*	X_5	X_4	X_3	X_2	X_1	X_0		Bank 0: X[5:0] = 31… 63; for pulse width set to 32 ~ 64 clocks (RESET = 110001b)
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		Color A: A[5:0] same as above (RESET = 111111b)
0	B[5:0]	*	*	B_5	B_4	B_3	B_2	B_1	B_0		Color B: B[5:0] same as above (RESET = 111111b)
0	C[5:0]	*	*	C_5	C_4	C_3	C_2	C_1	C_0		Color C: C[5:0] same as above (RESET =111111b) Note: color D pulse width is fixed at 64 clocks pulse.

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	92	1	0	0	1	0	0	1	0	Set bank color of for bank 1-16 (Page 0)	A[1:0] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 1
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[3:2] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 2
0	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		:
0	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		:
0	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		D[7:6]: 00, 01, 10, or 11 for Color = A, B, C or D of bank 16
0	93	1	0	0	1	0	0	1	1	Set bank color of for bank 17-32 (Page 1)	A[1:0] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 17
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[3:2] : 00, 01, 10, or 11 for Color = A, B, C or D of bank 18
0	B[7:0]	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0		:
0	C[7:0]	C_7	C_6	C_5	C_4	C_3	C_2	C_1	C_0		:
0	D[7:0]	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0		D[7:6]: 00, 01, 10, or 11 for Color = A, B, C or D of bank 32
0	A0~ A1	1	0	1	0	0	0	0	X_0	Set Segment Re-map **	X_0=0: column address 0 is mapped to SEG0 (RESET) X_0=1: column address 131 is mapped to SEG0
0	A4~A5	1	0	1	0	0	1	0	X_0	Set Entire Display ON/OFF **	X_0=0: normal display (RESET) X_0=1: entire display ON
0	A6~A7	1	0	1	0	0	1	1	X_0	Set Normal/Inverse Display **	X_0=0: normal display (RESET) X_0=1: inverse display
0 0	A8 A[5:0]	1 *	0 *	1 A_5	0 A_4	1 A_3	0 A_2	0 A_1	0 A_0	Set Multiplex Ratio **	The next command, A[5:0] determines multiplex ratio N from 16MUX-64MUX, RESET= 64MUX
0	AA	1	0	1	0	1	0	1	0	NOP	Reserved, do not use
0	AB	1	0	1	0	1	0	1	1	NOP	Reserved, do not use
0 **0**	**AD**	1 1	**0** **0**	1 **0**	**0** **0**	1 1	1 **0**	**0** 1	1 X_0	Set DC-DC on/off	X_0 : 1 DC-DC will be turned on when display on (RESET) 0 DC-DC is disable
0	AE~AF	1	0	1	0	1	1	1	X_0	Set Display ON/OFF **	X_0=0: turns OFF OLED panel (RESET) X_0=1: turns ON OLED panel
0	B0~BF	1	0	1	1	X_3	X_2	X_1	X_0	Set Page Address **	Set GDDRAM Page Address (0~7) for read/write using $X_3X_2X_1X_0$
0	C0/C8	1	1	0	0	X_3	*	*	*	Set COM Output Scan Direction **	X_3=0: normal mode (RESET) Scan from COM 0 to COM [N –1] X_3=1: remapped mode. Scan from COM [N-1] to COM0 Where N is the Multiplex ratio.
0	D0-D1	1	1	0	1	0	0	0	X_0	Reserved	Reserved, do not use

D/C	Hex	D7	D6	D5	D4	D3	D2	D1	D0	Command	Description
0	D3	1	1	0	1	0	0	1	1	Set Display Offset **	Set vertical scroll by COM from 0-63.
0	A[5:0]	*	*	A_5	A_4	A_3	A_2	A_1	A_0		The value is reset to 00H after RESET.
0	D5	1	1	0	1	0	1	0	1	Set Display Clock Divide Ratio/Oscillator Frequency	A[3:0] Define the divide ratio of the display clocks (DCLK):
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		Divide ratio= A[3:0] + 1, RESET is 0000b (divide ratio = 1) A[7:4] Set the Oscillator Frequency. Oscillator Frequency increases with the value of A[7:4] and vice versa. RESET is 0111b
0	D8	1	1	0	1	1	0	0	0	Set area color mode on/off & low power display mode	X_5X_4= 00 (RESET) : mono mode
0		0	0	X_5	X_4	0	X_2	0	X_0		X_5X_4= 11 Area Color enable X_2=0 and X_0=0: Normal (RESET) power mode X_2=1 and X_0=1: Set low power save mode
0	D9	1	1	0	1	1	0	0	1	Set Pre-charge period**	A[3:0] Phase 1 period of up to 15 dclk clocks [RESET=2h]; 0 is invalid entry
0	A[7:0]	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		A[7:4] Phase 2 period of up to 15 dclk clocks [RESET=2h]; 0 is invalid entry
0	DA	1	1	0	1	1	0	1	0	Set COM pins hardware configuration	X_4=0, Sequential COM pin configuration
0		0	0	0	X_4	0	0	1	0		(i.e. COM31, 30, 29….0 ; SEG0-132; COM31,32….62,63) X_4=1(RESET), Alternative COM pin configuration (i.e. COM62,60,58,…2,0; SEG0-132; COM1,3,5…61,63)
0	DB	1	1	0	1	1	0	1	1	Set VCOM Deselect Level	A[6:0] 0000000 low VCOM deselect level (~ 0.43 Vref)
0	A[6:0]	*	A_6	A_5	A_4	A_3	A_2	A_1	A_0		0110101 normal VCOM deselect level (~ 0.77*Vref (RESET)) 1111111 high VCOM deselect level (equal Vref)
0	E2	1	1	1	0	0	0	1	0	Reserved	Reserved
0	E3	1	1	1	0	0	0	1	1	NOP **	Command for No Operation
0	F*	1	1	1	1	*	*	*	*	Reserved	Reserved, do not use

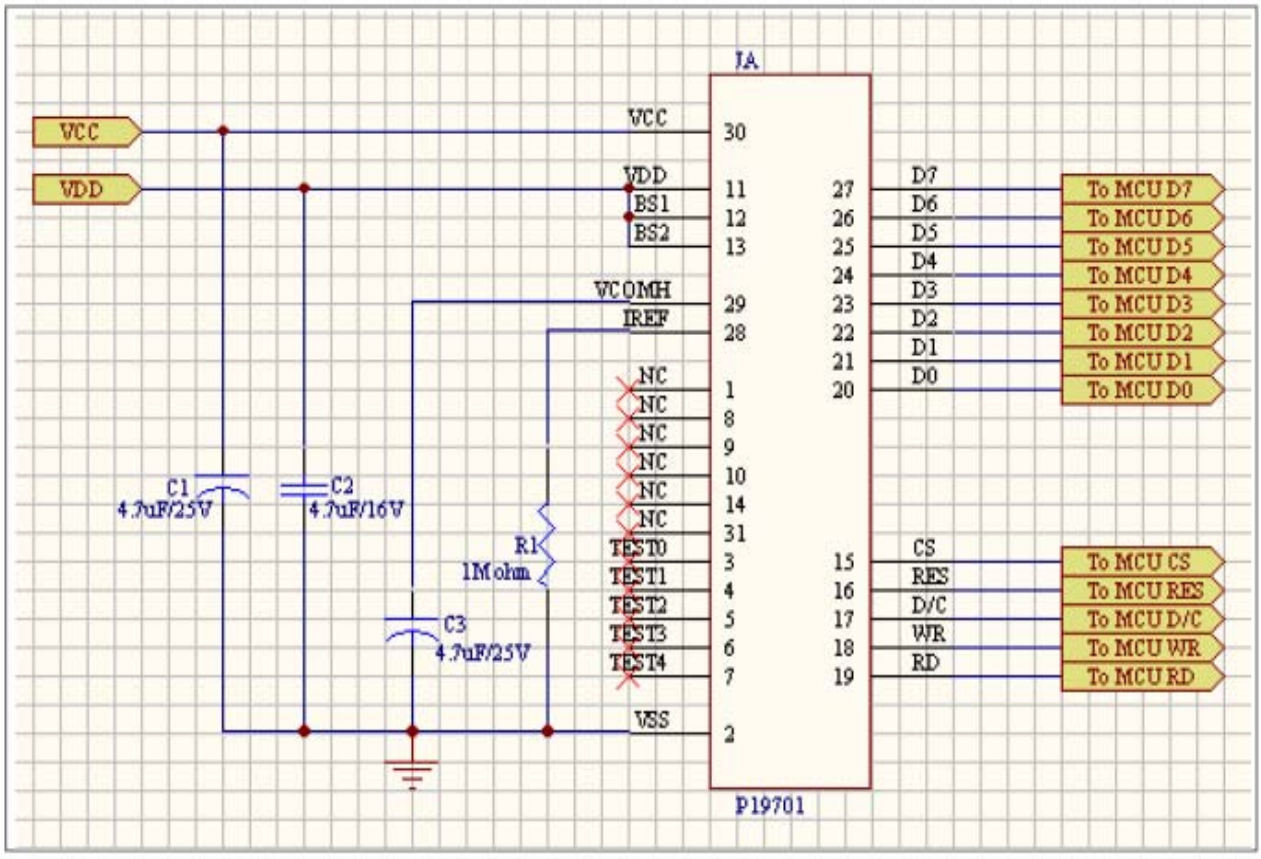
(D/C=0, R/W (WR#)=1, E (RD#)=1 for 6800 or E (RD#)=0 for 8080)

Bit Pattern	Command	Description
$D_7D_6D_5D_4D_3D_2D_1D_0$	Status Register Read *	D_7 : Reserve D_6 : "1" for display OFF / "0" for display ON D_5 : Reserve D_4 : Reserve D_3 : Reserve D_2 : Reserve D_1 : Reserve D_0 : Reserve

Note: Patterns other than those given in the Command Table are prohibited to enter the chip as a command; as unexpected results can occur.

10 Application

10.1 Application Circuit



Recommended components

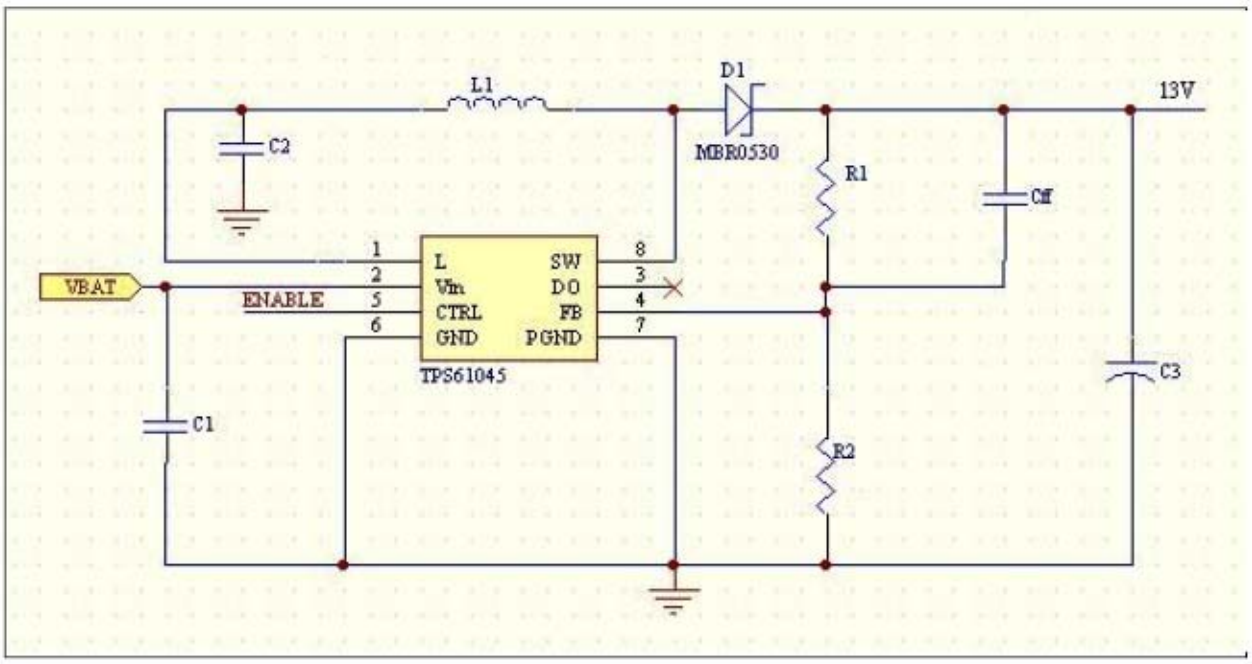
R1 : 1M ohm (0603),1%.

C1 : 4.7uF (Tantalum Type) / 25V, C2 : 4.7uF (0805) / 16V ,

C3 : 4.7uF (Tantalum Type) / 25V.

This circuit is designed for 8080 8-bits interface.

10.2 External DC-DC application circuit



Recommended components

C1: 0.1uF(0603) / 25V, C2 : 4.7uF (Tantalum Type) / 25V,

C3 : 4.7uF (Tantalum Type) / 25V.

Cff : 22pF(0603) / 16V.

D1:Schotty Diode.

L1: 10uH.

R1: 1.2M ohm (0603), 1%, R2: 127K ohm (0603), 1%.

VBAT = 1.8V ~ 6.0V(The Detail Application,please refer the IC data sheet).

10.3 Initial software

```
void OM_ini()
{
    write_com(0xae);      //Set Display ON/OFF
    write_com(0xad);      //master configuration
     write_com(0x8a);      //second byte
    write_com(0xa8);      //Set Mux
     write_com(0x3f);      //64mux
    write_com(0xa0);      //Set Segment Re-map (0xa0 normal,0xa1 reverse)
    write_com(0xc8);      //Set COM Output Scan Direction (0xc0 normal,0xc8 reverse)
    write_com(0xa6);      //set normal/inverse display (normal)
    write_com(0xa4);      //set entire display (normal)
    write_com(0x81);       //set contrast control
     write_com(0x8f);   //second byte
    write_com(0xd5);      //Set Display Clock Divide Ratio/Oscillator Frequency
     write_com(0x70);     //105hz
    write_com(0xd8);      //Set Area Color Mode ON/OFF & LowPower Display Mode
     write_com(0x00);      //second byte
    write_com(0xd9);      //set pre-charge period
     write_com(0x61);   //set discharge/precharge
    write_com(0xaf);      //Set Display ON
}
```

11 Precautions for operation and Storage

11.1 Precautions for Operation

(1) Since OLED panel is made of glass, in order to prevent from glass broken, please do not apply any mechanical shock or impact or excessive force to it when installing the OLED module. Any strong mechanical impact due to falling dropping etc. may cause damage (breakage or cracking).

(2) The polarizer on the OLED surface is made of soft material and is easily scratched. Please take most care when handing.

(3) If OLED surface is contaminated, please wipe it off gently by using moisten soft cloth with normal ethanol, do not use acetone, ketone, isopropyl alcohol or water. If there is saliva or water on the OLED surface, please wipe it off immediately.

(4) When handling OLED module, please be sure that the body and the tools are properly rounded. And do not touch I/O pins with bare hands or contaminate I/O pins, it will cause disconnection or defective insulation of terminals.

(5) Do not attempt to disassemble or process the OLED module.

(6) OLED module should be used under recommended operating conditions shown in the specification. Since the higher voltage leads to the shorter lifetime, be sure to use the specified operating voltage.

(7) Foggy dew, moisture condensation or water droplets deposited on surface and contact terminals will cause polarizer stain or damage, the deteriorated display quality and electrochemical reaction then leads to the shorter life time and permanent damage to the module probably. Please pay attention to the environmental temperature and humidity.

11.2 Soldering

(8) Use the high quality solder. (60-63% tin mixed with lead)

(9) Iron: no higher than 260℃ and less than 3~4 sec during soldering.

(10) Soldering: only to the I/O terminals.

(11) Rewiring: no more than 3 times.

11.3 Precautions for Storage

(12) Please store OLED module in a dark place, avoid exposure to sunlight, the light of fluorescent lamp or any ultraviolet ray.

(13) Keep the environment temperature at between 10°C and 35°C and the relative humidity less than 60%. Avoid high temperature, high humidity.

(14) That keeps the OLED modules stored in the container shipped from supplier before using them is recommended.

(15) Do not leave any article on the OLED module surface for an extended period of time.

11.4 Warranty period

Multi-Inno Technology Co. Ltd. warrants for a period of 12 months from the shipping date when stored or used under normal condition

12 Test Status

TEST ITEM	TEST CONDITION	QUANTITY
High temperature storage	85°C,120 hours	3pcs
Low temperature storage	-40°C,120 hours	3pcs
Humidity (storage)	60°C, 90%RH, 120hours	3pcs
Low temperature (operating)	-40°C, 120 hours	3pcs
High temperature (operating)	80°C, 120hours	3pcs

Note: After test 2 hours (room temperature), check function & appearance.